BMS
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

BASIC ELECTRONICS

18ELN14/24

STUDY MATERIAL

I/II SEMESTER

Question Bank:

MODULE-1
Semi Conductor Diodes and its Applications

Topic 1. PN junction Diode

- **P-N Junction Diode Construction**
- **Working of P N junction diode under FB & RB**
- **Equivalent Circuit**
- **Problems**

Topic 2 Rectifiers Circuit

- **Working of HW,FW and BW rectifiers circuit along with input output waveform (like plot of $V_{secondary}$, I_L, V_{dc}, V_L, Load current during +ve and –ve half cycle of supply)**
- **HWR with C filter**
- **Derivation of I_{dc}, I_{rms}, V_{dc}, V_{rms}, ripple factor, efficiency of HW, FW,BWR.**
- **Advantages & Disadvantages of HW,FW,BWR**
- **Comparison of HW, FW and BWR.**
- **Problems**

Topic 3. Zener Diode

- **Zener Diode and its I-V Characteristics**
- **Zener Diode as a Voltage regulator (line/voltage regulation and Load Regulation)**
- **Problems**

Topic 4 Special Diodes

- **Photo Diode (working, V-I characteristics, Advantages, Disadvantages and Applications)**
- **LED (working, V-I characteristics, Advantages, Disadvantages and Applications)**
- **Photo Coupler (working, Advantages, Disadvantages and Applications)**

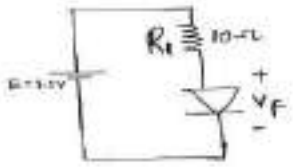
Topic 5 Fixed Voltage Regulators

- **Block diagram of three terminal fixed voltage regulator**
- **Functional Block diagram of 78XX/7805 series three terminal IC regulator.**

Topic 1. PN junction Diode

- **P-N Junction Diode Construction**
- **Working of P N junction diode under FB & RB**
- **Equivalent Circuit**
- **Problems**

1. Explain the working of PN junction diode under forward and reverse biased conditions. (06 Marks) Dec/ Jan 2018/ Dec /Jan 2020/ MQP1/MQP2
2. What is semiconductor diode ? Explain the different Circuits of diode. (06 Marks) June /July 2019
3. A diode circuit shown below has E=1.5V, R_1=10 ohm. By assuming V_f =0.7V, calculate If for i) rd = 0 ii) rd = 0.25 ohm (MQP1)



Topic 2 Rectifiers Circuit

- **Working of HW,FW and BW rectifiers circuit along with input output waveform (like plot of $V_{secondary}$, I_L, V_{dc}, V_L, Load current during +ve and –ve half cycle of supply)**
- **HWR with C filter**
- **Derivation of I_{dc}, I_{rms}, V_{dc}, V_{rms}, ripple factor, efficiency of HW, FW,BWR.**
- **Advantages & Disadvantages of HW,FW,BWR**
- **Comparison of HW, FW and BWR.**
- **Problems**

1. Explain with neat circuit diagram and waveforms the working of center-tap full wave rectifier. Show that efficiency of full-wave rectifier is 81%. (08 Marks)/ Dec/ Jan 2018/ Dec-Jan 2020

2. Explain the operation of half wave rectifier with capacitor filter with neat circuit diagram and waveform. (06 Marks)/ Dec/ Jan 2018/ Dec-Jan 2020/ (MQP1)

3. Show that the ripple factor of a half wave rectifier is 1.21 and efficiency is 40.5%. (06 Marks)/ Dec/ Jan 2018.

4. With a neat circuit diagram and waveforms, explain the working of full wave bridge rectifier. Also derive Vdc, Vrms values for Full wave rectifier. (09 Marks) June /July 2019

5. A full wave rectifier uses 2 diodes having internal resistance of 20Ω each. The transformer rms secondary voltage from centre to each end is 50v. Find Im, Idc, Irms and Vdc if the load is 980Ω . (06 Marks)/June /July 2019 .

6. A full wave rectifier uses 2 diodes having internal resistance of 10Ω each. The transformer rms secondary voltage from centre to each end is 200v. Find Im, Idc, Irms and Vdc if the load is 800Ω . (06 Marks) Dec-Jan 2020.

7. With a neat circuit diagram and waveform, explain the working of half-wave rectifier and derive the expression for average load current. (MQP1)

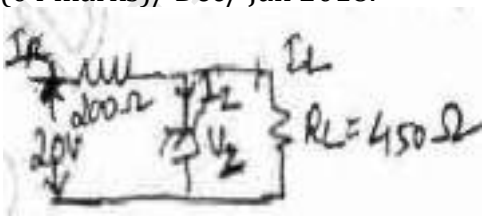
8. full wave bridge rectifier with an input of 100V(rms) feeds a load of 1kΩ .VΩ .VT=0.7V
   (i) If the diodes employed are of silicon, what is the dc voltage across the load?
   (ii) Determine the PIV rating of each diode..
   (iii) Determine the maximum current that each diode conducts and the diode power rating. (MQP2)

9. A half wave rectifier is fed from a supply of 230 V, 50 Hz with step down transformer of ratio 3:1. Resistive load connected is 10 KΩ. The diode forward resistance is 75Ω and transformer secondary is 10 Ω. Calculate the DC load current, DC load voltage, efficiency and ripple factor. (MQP3)

Topic 3. Zener Diode

- **Zener Diode and its I-V Characteristics**
- **Zener Diode as a Voltage regulator (line/voltage regulation and Load Regulation)**
- **Problems**

1. Explain how zener diode helps in voltage regulation with neat circuit diagram. Give detail mathematical analysis. (06 Marks)/ Dec/ Jan 2018/ (08 Marks) June -July 2019/ Dec-Jan 2020/MQP1
2. For the circuit shown in Fig. Find the current and voltage in the circuit for $R_L = 450\Omega$. (04 marks)/ Dec/ Jan 2018.



3. A Zener diode has a breakdown voltage of 10V. It is supplied from a voltage source varying between 20-40V in series with a resistance of 820Ω. Using an ideal Zener model, obtain the minimum and maximum Zener currents (MQP3)

Topic 4 Special Diodes

- **Photo Diode (working, V-I characteristics, Advantages, Disadvantages and Applications)**
- **LED (working, V-I characteristics, Advantages, Disadvantages and Applications)**
- **Photo Coupler (working, Advantages, Disadvantages and Applications)**

1. Explain VI characteristics of Photodiode and its operation. (04 marks)/ Dec/ Jan 2018/ June -July 2019/ (5Marks) Dec-Jan 2020.\
2. Write a short note on
   (i) Light emitting diode and (ii) Photo coupler (MQP2)

Topic 5 Fixed Voltage Regulators

- **Block diagram of three terminal fixed voltage regulator**
- **Functional Block diagram of 78XX/7805 series three terminal IC regulator**

1. Explain the functional Block diagram of 78XX series voltage regulator. (06Marks)
2. Explain the operation of 7805 fixed IC voltage regulator. (MQP1)
3. Explain the features of LM7805 fixed regulator. (MQP 3)

Question Bank

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MODULE-2

FET and SCR

Introduction, JFET: Construction and operation, JFET Drain Characteristics and Parameters, JFET Transfer Characteristics, Square Law expression for I_D, Input resistance.

MOSFET: Depletion and Enhancement type MOSFET-Construction, Operation, Characteristics and Symbols (7.1,7.2,7.4,7.5 of Text 2),

CMOS (4.5 of Text 1).

Silicon Controlled Rectifier (SCR)- Two transistor model, switching action, characteristics, phase control application (3.4 to 3.4.5 of Text 1)

1. Text 1 : D.P Kothari, I.J Nagarath, "Basic Electronics", 2nd edition, Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

Topic 1. JFET

1. Explain the drain and transfer characteristics of a JFET with neat circuit diagram **(08 Marks) Dec 2018-Jan 2019.**
2. Explain the basic structure and operation of JFET with neat diagram. (08 Marks) **Dec 2018-Jan 2019.**
3. For a JFET I_{DSS}=9mA and $V_{GS(off)}$=-8 $V_{(max)}$ determine drain current for V_{GS}= -4volts. **(04 Marks) Dec 2018-Jan 2019.**
4. For a N-channel JFET if I_{DSS}=8mA and V_p= -5volts, calculate I_D at V_{gs}=-3volts and V_{gs} at I_D=3mA. **(05 Marks) June-July 2019.**
5. Explain the construction, working and characteristics of N-channel JFET. **(05 Marks) June-July 2019/(06 Marks) Dec2019-Jan 2020/ (8 Marks) MQP-1/(7 Marks)MQP-2./ (6 Marks)MQP-3.**
6. For a N-channel JFET if I_{DSS}=9mA and V_p= -6volts, calculate I_D at V_{gs}=-4volts and V_{gs} at I_D=3mA. **(05 Marks) Dec2019-Jan 2020.**
7. A certain JFET has an I_{GSS} of -2nA for V_{GS} = -20V. Determine the input resistance. **(4 Marks) MQP-2**
8. Explain the construction and operation of a p-channel JFET. **(8 Marks)MQP-3**

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Topic 2. MOSFET

1. Explain the operation of an enhancement MOSFET with neat circuit diagram. **(06 Marks) Dec 2018-Jan 2019.**
2. Explain the construction, working and characteristics of enhancement type MOSFET. **(09 Marks) June-July 2019./ (09 Marks) Dec2019-Jan 2020/(8 Marks)MQP-3.**
3. For an EMOSFET, determine the value of I_D if $I_{D(on)}$=4mA, $V_{gs(on)}$=6volts, V_T=4volts and V_{gs}= 8volts. **(05 Marks) Dec2019-Jan 2020./(4Marks)MQP-1.**
4. Explain the construction and working of P-channel enhancement type MOSFET. **(8 Marks) MQP-1.**
5. What is MOSFET? Explain D-MSFET and E-MOSFET transfer characteristics. **(8 Marks)MQP-2**

Topic 3. CMOS

1. Explain CMOS as an inverter with neat circuit diagram. Give its equivalent circuit and its advantages. **(08 Marks) Dec 2018-Jan 2019.**
2. With a neat circuit diagram explain the working of CMOS inverter. **(06 Marks) June-July 2019./ (06 Marks) Dec2019-Jan 2020./ (6 Marks)MQP-1./ (7 Marks)MQP-2/(6 Marks)MQP-3**

Topic 4. SCR

1. Explain VI characteristics of SCR. **(06 Marks) Dec 2018-Jan 2019./ (6 Marks)MQP-2/(6 Marks)MQP-3**
2. What is SCR ? Explain the working of SCR using two transistor model. **(06 Marks) June-July 2019./ (06 Marks) Dec2019-Jan 2020./ (8Marks)MQP-1./ (6 Marks)MQP-2/(6 Marks)MQP-3**
3. What is commutation in SCR? Explain two types of communication. **(05 Marks) June-July 2019.**
4. Explain phase controlled application of SCR. **(6 Marks)MQP-1.**

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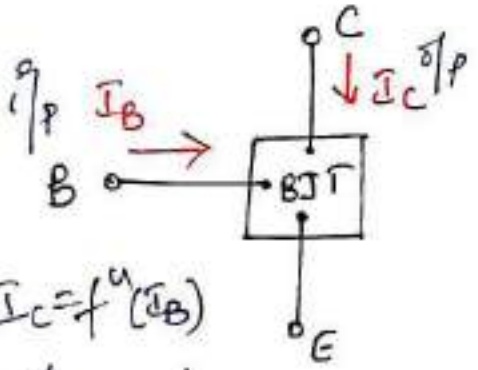
Introduction to Field-Effect Transistor

FETs with BJTs

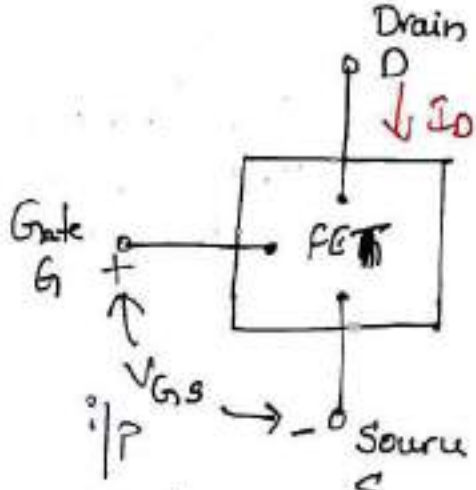
* Like BJT, FET is also 3 terminal device



$I_C = f^n(I_B)$

- o/p current I_C is controlled by i/p current I_B

$$I_C = \beta I_B$$



$I_D = f^n(V_{GS})$

- o/p current I_D is controlled by i/p voltage V_{GS}.

* Application of FET ≅ Application of BJT.

* BJT is a Current Controlled device

$I_C = f^n(I_B)$ ← i/p current.

* FET is voltage Controlled device.

$I_D = f^n(V_{GS})$ ← i/p voltage

→ BJT is a Bipolar device :- charge carriers are both electrons (e⁻) and holes.

FET is a Unipolar device :- But here charge carriers are either electrons (e⁻) (or) holes.

A1

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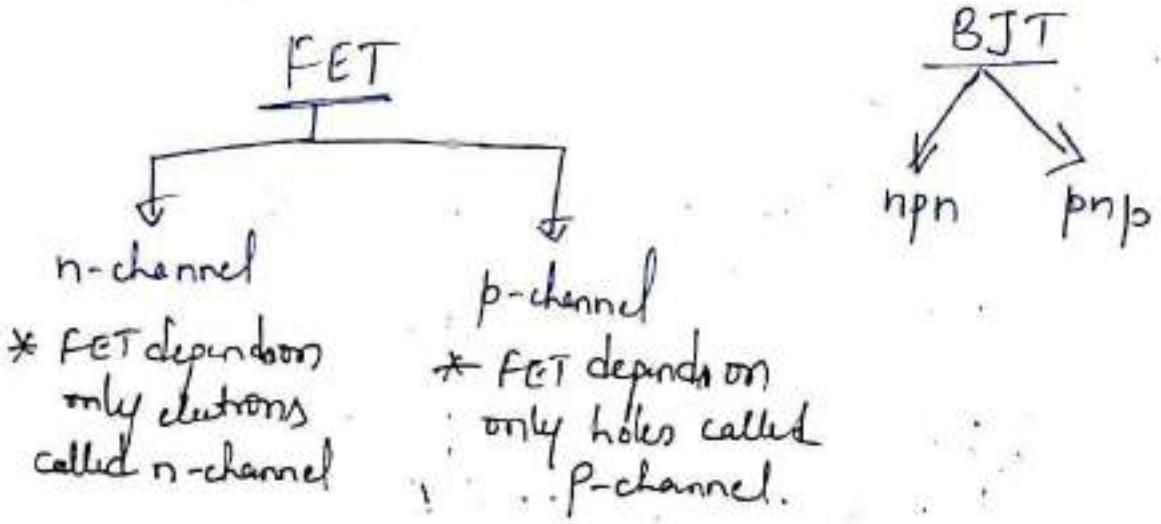
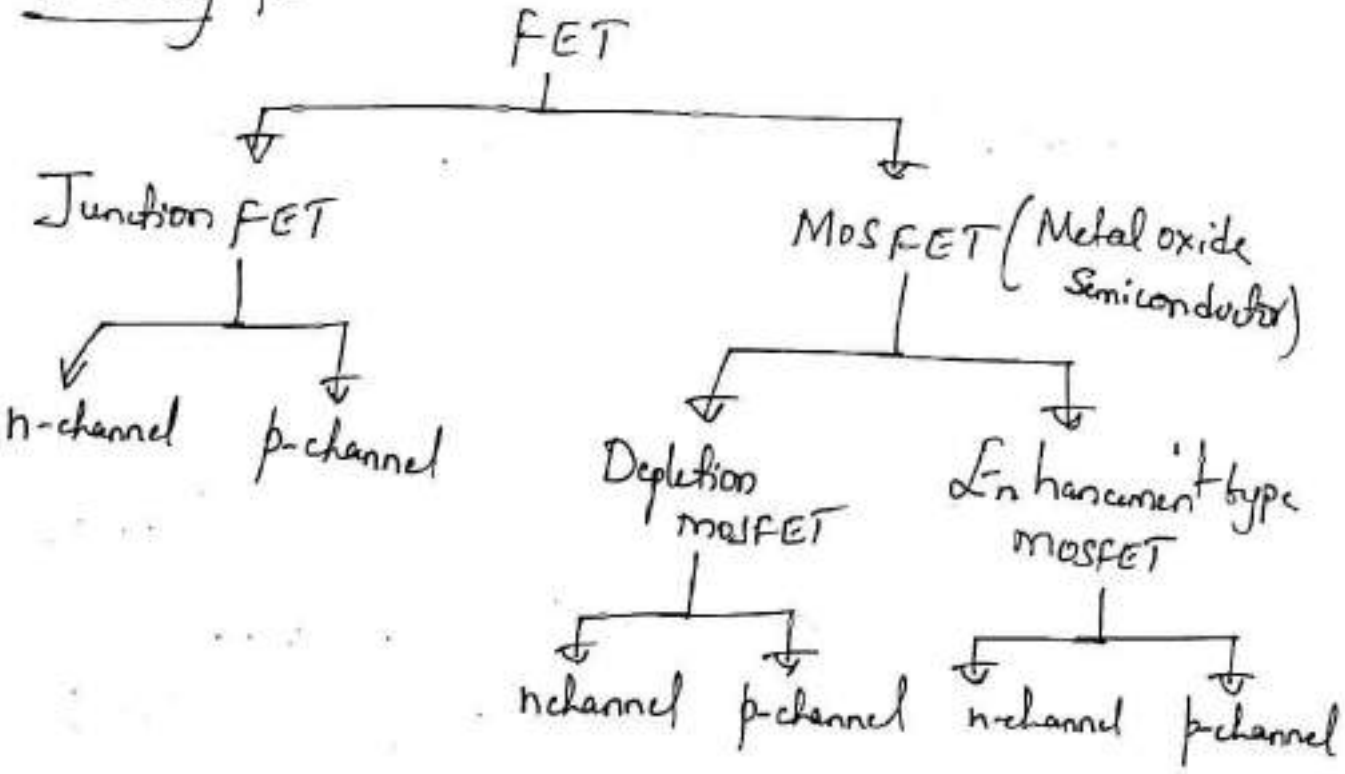
Classification.



* FET can be used for both Amplification and Switching like BJT.

* Hierarchy of



A2

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History of FET

* the FET was first patented by "Julius Edger Lilien field" 1926. and By oskar Heil in 1934. } not actual FET but concepth like FET

and MOSFET which is Botterthan FET was invented by "D.kahng" in 1959.

Meaning of "Field-effect" in FET.

* In case of FET an electric field is developed by the charges present and this "electric field" controls the conduction path of the output circuit.

i/p impedance:-

↳ FETs have Z_i ↑ Compared to BJT.

* FETs are More Temperature stable compared BJT.
* FETs are Smallerthan (Size) BJTs.
* BJTs are More Sensitive to the applied Signals Compared to the FETs.

A3

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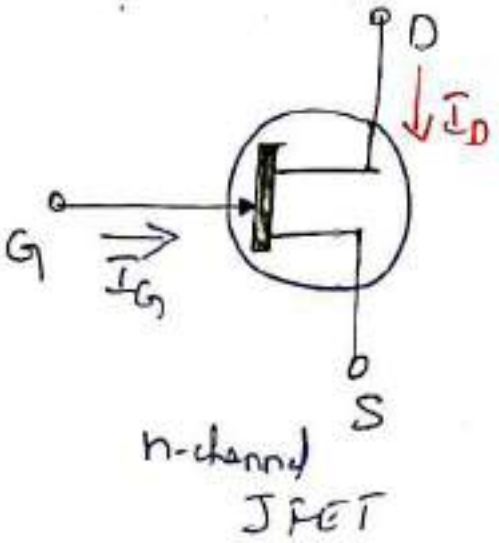
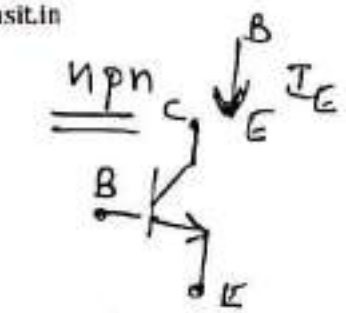
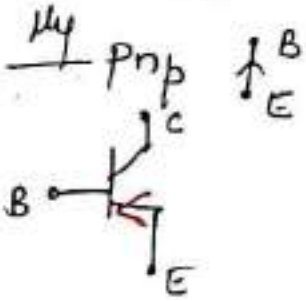
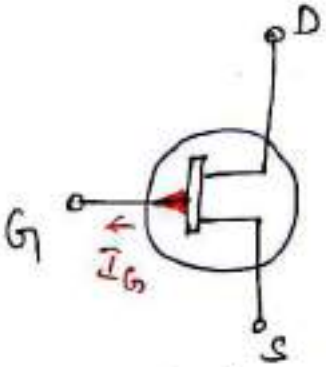
Symbol:-



n-channel JFET







p-channel JFET

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MODULE-2
Topic 1. JFET

Explain the construction, working and characteristics of N-channel JFET. **(05 Marks) June-July 2019/(06 Marks) Dec2019-Jan 2020/ (8 Marks) MQP-1/(7 Marks)MQP-2./ (6 Marks)MQP-3.**

Explain the basic structure and operation of JFET with neat diagram. **(08 Marks) Dec 2018-Jan 2019.**

Soln:-

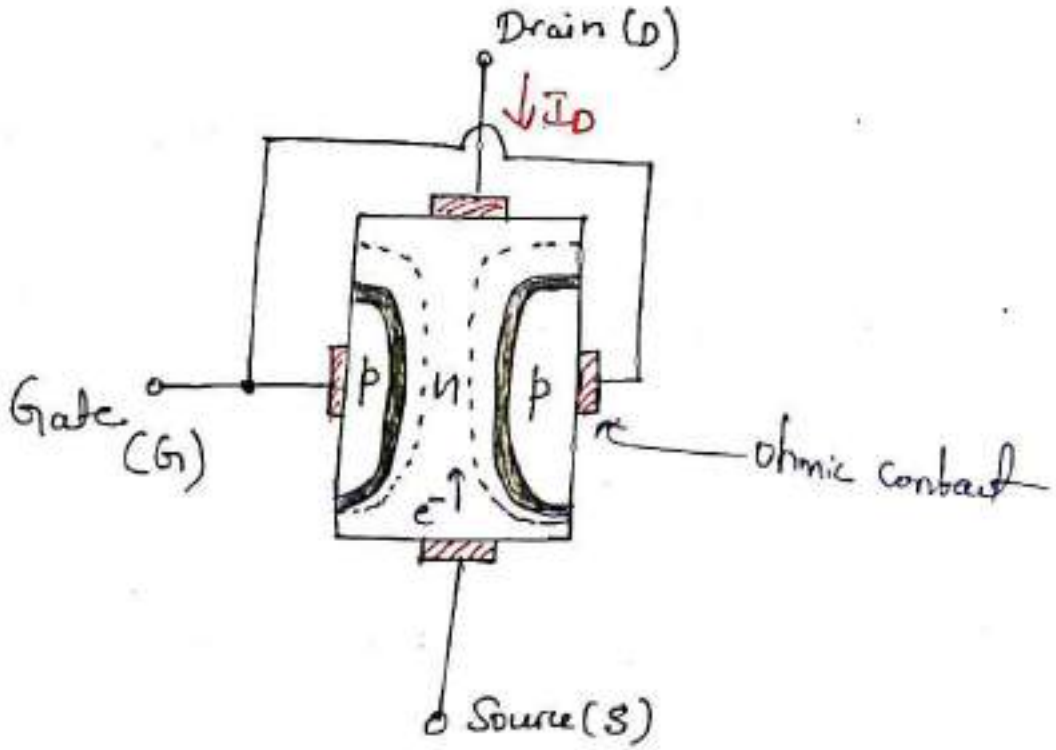

fig:- n-channel JFET.

Construction:-

* Fig. shows the construction of n-channel JFET. the major part of JFET structure is n-type material and it is forming channel between two embedded p-type material.
* n-type material forming channel blw two p-type Material by this reason, we call it is n-channel JFET.

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* There are four ohmic contacts and three terminals namely Gate (G), Source (S) and Drain (D).

* There are two p-N junctions formed b/w p type and N-type material. Results two Depletion regions are formed. [In depletion region no free charge carriers].

* if Width of Depletion Layer increases, if results width of n-channel decreases, bcz of this there is an obstruction in flow of Current.

* the Width of depletion region is controlled by Gate (G) terminal.
i.e potential difference b/w Gate & Source terminal "V_{GS}" Controls the Drain current (I_D).

⇒ The output current (I_D) is controlled by input voltage (V_{GS}) ∴ FET is an "voltage controlled device.

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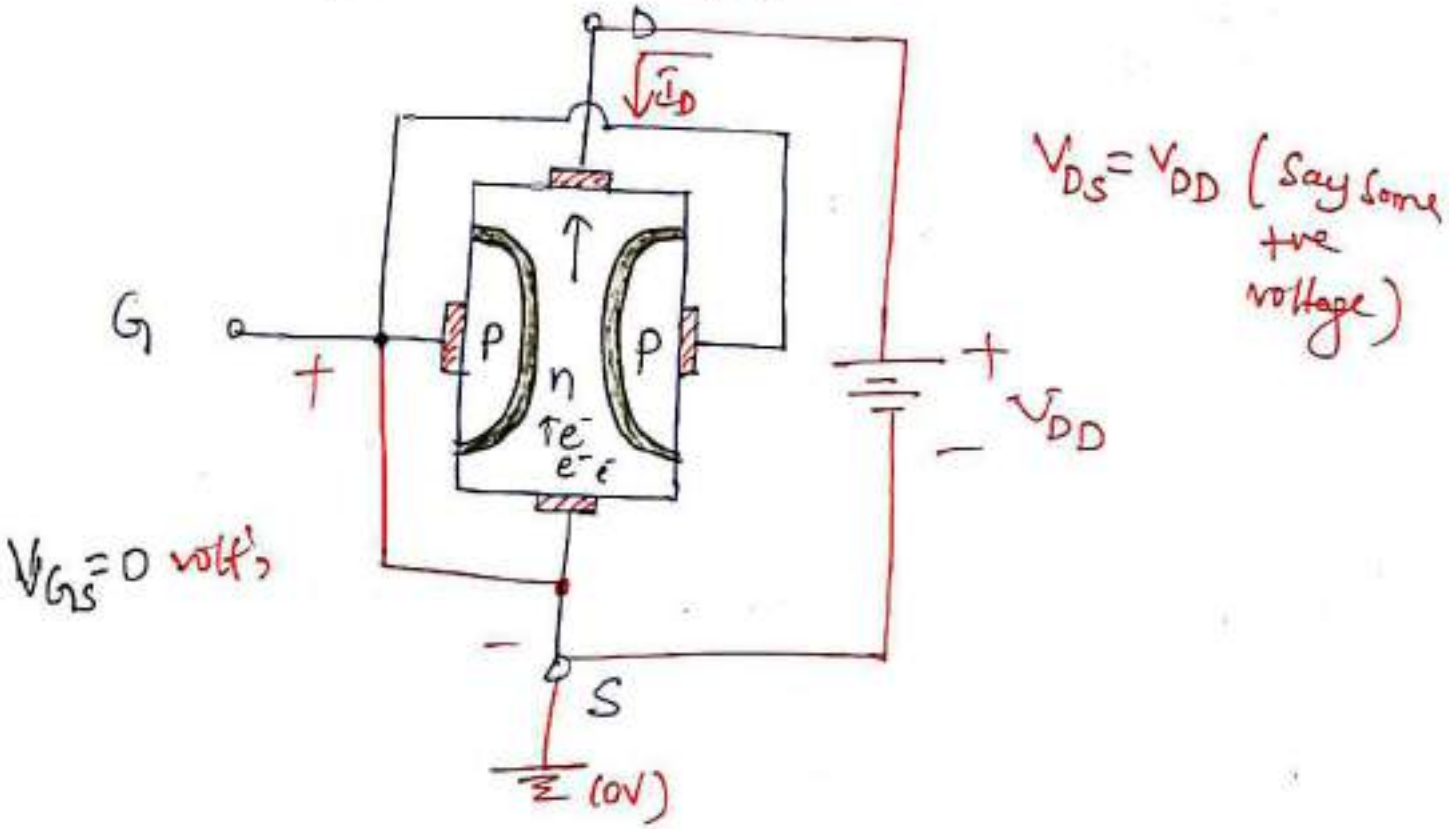
Working of JFET :-

Case i: $V_{GS} = 0V$ and $V_{DS} > 0V$.

Case ii: $V_{GS} < 0V$.

Case i: $V_{GS} = 0V$ and $V_{DS} > 0V$.



* Because of the applied external potential (V_{DD}), the electrons in a n-channel drift's easily from Source to drain. results drain Current I_D.

* Depletion Layer :- Since $V_{DS} = V_{DD}$ (+ve) width of depletion region changes.

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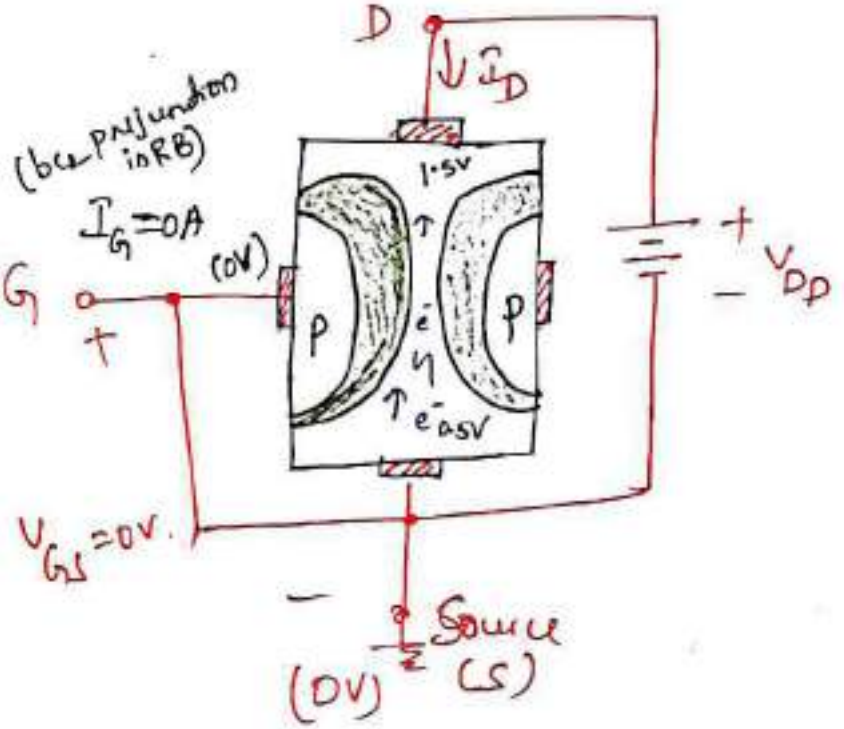
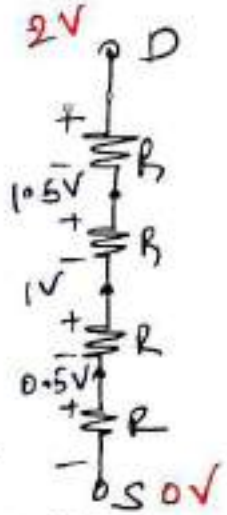
→ The width of the depletion region is almost same in the bottom but it will increase at the top.



Reason: n-channel providing resistance for current flow (I_D).

Consider n-channel as four resistance



Eg: V_{DD} = +2V

R_{eq} = 4R.

2V → 4R

∴ Each R = 0.5Volt's voltage is

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* at the top applied Reverse bias voltage is more ; the depletion region is increases. but at bottom the applied Reverse bias voltage is very less ; the width of depletion region is almost same.

* The Gate current $I_G = 0A$. bcz pn junction is Reverse biased.

Pinch-off Voltage :-

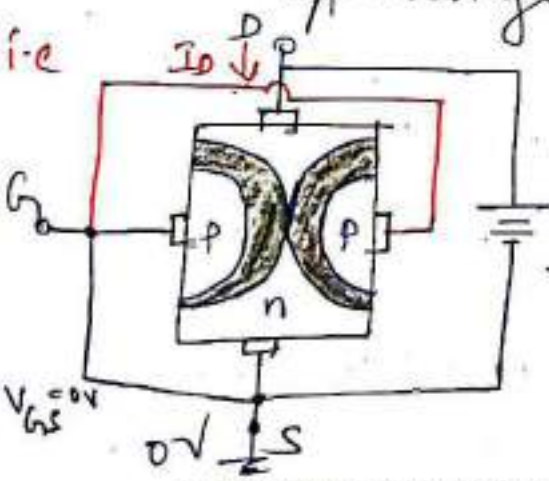
$V_{GS} = V_G - V_S$

When $V_{GS} = 0$ V and $V_{DS} = V_{DD} > 0$V (+ve)

An increasing $V_{DS} = V_{DD} \uparrow$, the Current $I_D \uparrow$ and also the two Width of the depletion layer's also increases touching each other.

and the Corresponding voltage V_{DS} is called pinch -off voltage. (V_P)

i.e



Pinch off voltage :- if V_{DS} is increased to a level where both the depletion layer's touchs each other, the Condition is called pinch-off and the corresponding voltage V_{DS} is called pinch-off voltage.

Ag

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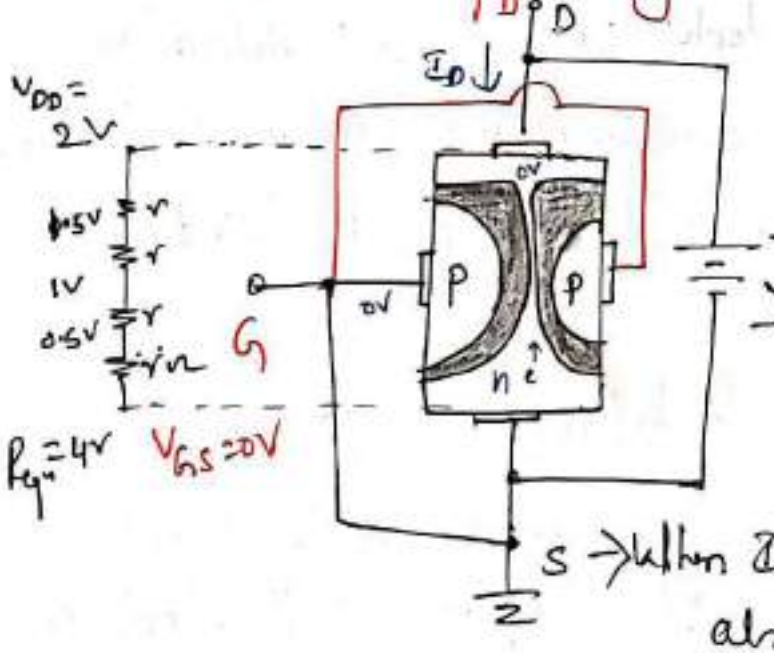
$V_{DS} = V_{DD} \uparrow \Rightarrow$ two Depletion region touch each other the Corresponding voltage V_{DS} is called "Pinch-off voltage".

the pinch off voltage is denoted by (V_p).

Note:- But in Reality the two depletion region's will never touch Each other. the channel in still ther but width is very small. bcz of thin the current density will increase.

Reason for two depletion regions not touches Eachother:-



When $V_{DD} \uparrow \Rightarrow$ depletion region touches $\Rightarrow I_D = 0$ but in reality $I_D \neq 0$ bcz of voltage drop across the resistances.

S → When $I_D = 0$. drop across resistors also equal to '0'. result's

∴ PN is not under reverse bias

∴ two depletion region's not touches each other.

Aq

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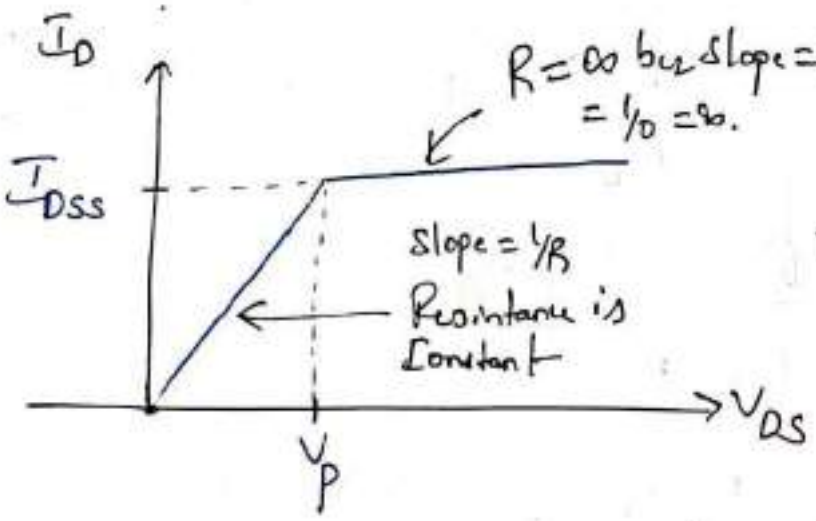
I_D Vs.
plot Graph b/w voltage (V_{GS})



* I_{DSS} :- Maximum drain current, when V_{GS} = 0 volts and $V_{DS} > |V_p|$

Drain to Source current — but V_{GS} = 0 V.

* Depletion layer ? and I_D = ? when $V_{DS} > V_p$.

effect on

i.e

JFET as a Current Source :-

when $V_{DS} > V_p$.

* the width of depletion region will not increase at the top but it will increase at the bottom along with the length of channel.

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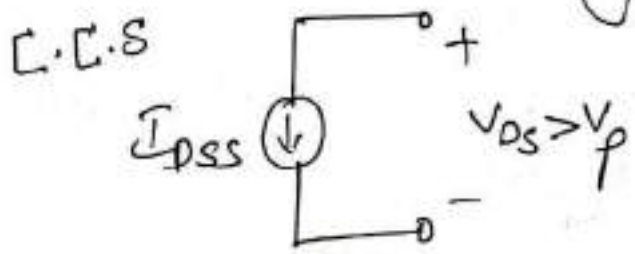
→ when $V_{DS} > V_p$ ⇒ $\boxed{I_D = I_{DSS}}$ true when only $V_{DS} < V_{DS(maximum)}$.

at this Condition JFET acting as Constant Current Source.



Case(ii) Working of JFET (Negative voltage at GATE)

i.e $V_{GS} < 0V$ and $V_{DS} = V_{DD}' < V_{DD}$.

(negative) (prime)

To obtain the Saturation at Lower value of V_{DS}

I_D → remains constant - with change in V_{DS}.

Case i

$V_{GS} = 0V$ and $V_{DS} = V_{DD} > 0V$

@ $V_{DS} > |V_p|$

$I_D = I_{DSS}$ (Maximum).

But

Case ii $V_{GS} < 0V$.

and $V_{DS} = V_{DD}' < V_{DD}$.

I_D → Constant but not I_{DSS} X. (not a Maximum)

ie to obtain Saturation Current at Lower Value of V_{DS}.

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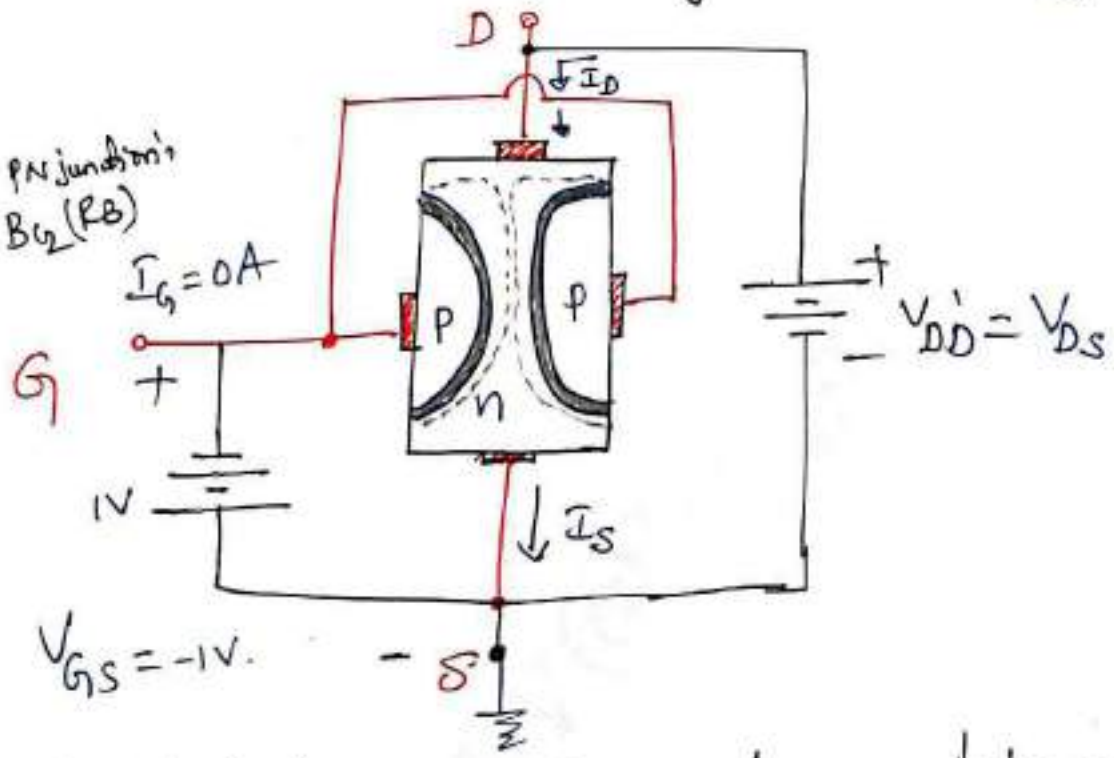
Obtain the saturation at Lower value of V_{DS}.

i.e $V_{DS}\downarrow$ by making V_{GS} is More negative.



* Width of depletion region increases because p-type material is connected to Lower potential and n-type is connected to higher potential.
* as $V_{DD}\uparrow$ both the depletion regions are touches Each other say at voltage $V_{DD} = V_P$.

the V_P in case(ii) is Lower compared to case(i).

bc_2 Gate is negatively biased. and.

* if $V_{DD} > |V_P| \Rightarrow I_D \rightarrow$ "Constant" (Saturation Current).

Note:- By applying -ve bias to the Gate, Saturation level can be reached at the Lower level of V_{DS}.

A12

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Explain the drain and transfer characteristics of a JFET with neat circuit diagram **(08 Marks)** **Dec 2018-Jan 2019.**

Soln:- (a) Output (or) Drain Characteristics of JFET.

JFET

I_D v/s V_{DS}

I_D ↑ o/p current

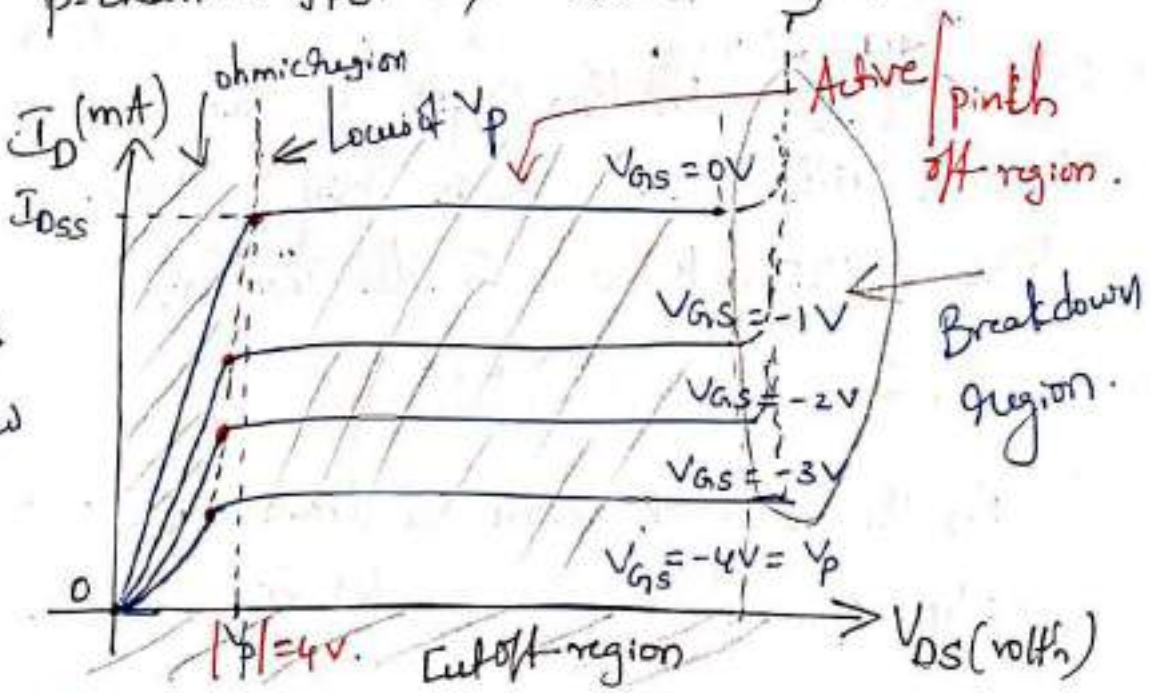
V_{DS} ↑ o/p voltage.

for different Levels V_{GS} (i/p voltage).
(or) control i/p.

In general

n-channel JFET $\Rightarrow V_{GS} < 0V$.

p-channel JFET $\Rightarrow V_{GS} > 0V$.



$I_{DSS} = 8mA$ → cond^n to Obtain $V_{GS} = 0V$. & $V_{DS} > |V_p|$.

$V_p = -4V$ @ $V_{GS} = 0V$, $I_D = I_{DSS}$

& $V_p = V_{DS}$

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When $V_{GS} < 0$ V.

By making V_{GS} more - and More negative.

n channel → +ve
P-type → -ve
} Reverse Baise ↑ ⇒ Width of depletion region ↑

∴ pinch off Voltage at the Lower value of V_{DS}

* Fig. shows the drain Characteristics of a n-channel JFET. The curves represent relationship b/w drain Current (I_D) and drain-Source voltage (V_{DS}) for different values of V_{GS}.

i. Ohmic Region :- In this region the drain Current (I_D) increases Linearly with the increase in drain to Source voltage (V_{DS}). here JFET acts as a Simple Resistor.

ii. Saturation Region (or) Pinch off region :-

In the saturation region the drain Current I_D remains fairly constant and doesnot vary with V_{DS}.

iii. Cutoff region :- $V_{GS(off)} = -V_p$ the value of $I_D = 0$A.

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iv. Breakdown Region:- $V_{DS} > (V_{DS})_{max}$.

In this region the drain current increases rapidly as the drain to Source voltage (V_{DS}) increases. This happens because of breakdown of gate to Source junction due to avalanche breakdown.

Note:- Pinch-off voltage (V_p):-

i. The voltage V_{DS} at which the current I_D reaches to its Constant saturation level is called "pinch off voltage" (V_p).

i.e $V_{GS}=0$, $V_{DS}=|V_p| \Rightarrow I_D = I_{DSS}$ (Maximum).

ii. By making V_{GS} more negative (i.e $V_{GS}<<0$), the pinch-off voltage is reached at lower values of I_D.

AS

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ii. Transfer characteristics of JFET

* In case of JFET, Transfer characteristics is a plot of I_D v/s V_{GS} plot by keeping V_{DS} → Constant.

(I_D → o/p, V_{GS} → i/p, V_{DS} → o/p voltage)

* $I_D = f^n(V_{GS})$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

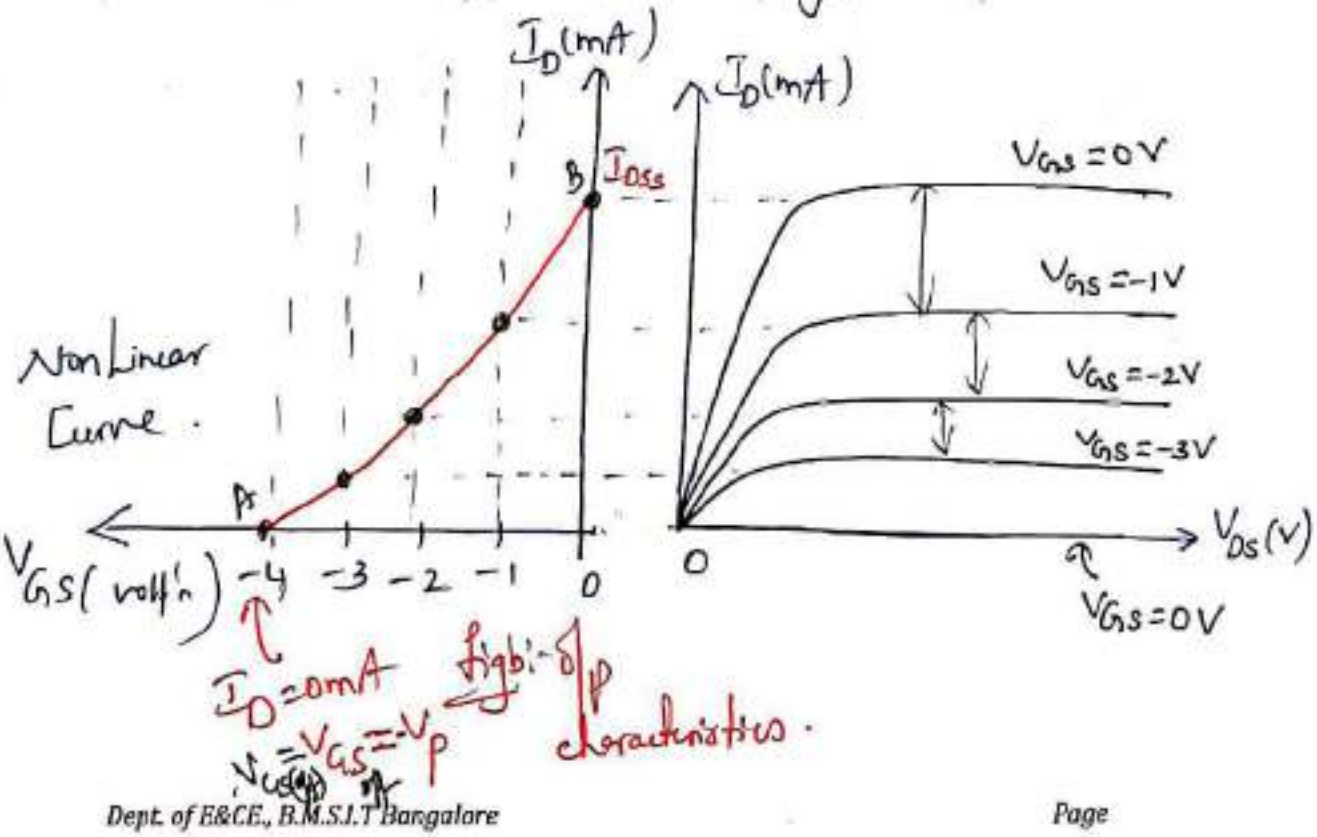
I_D → Controlling i/p

Square law expression.

Non Linear eq^n.

I_{DSS} → Constant

$V_{GS} \downarrow \Rightarrow I_D \uparrow$ (Exponentially)



A16

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* Square Law Expression for I_D.

The relationship between the drain current I_D and gate Source voltage (V_{GS}) is non Linear as shown in fig (b). This relation is defined by shockley's equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \longleftarrow (1)$$

Here I_{DSS} & V_p are Constant and V_{GS} is controls the I_D.

$\Rightarrow$ from eq^n (1) $V_{GS} = V_p\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$

* at point A i.e at the bottom end of the curve on the V_{GS} axis represents $V_{GS(off)}$, and point B at the top end of the curve on the I_D axis represents I_{DSS} (Maximum drain current at $V_{GS} = 0V$). Thus this curve shows the operating Limits of a JFET.

i.e $I_D = 0A$; when $V_{GS} = V_{GS(off)} = -V_p$.

$I_D = I_{DSS}$: when $V_{GS} = 0$ Volts.

A17.

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Problem:

The device parameters for n-channel JFET are:
Maximum drain current (I_{DSS}) = 10mA.
Pinch-off voltage (V_P) = -4V.
Calculate the drain current for
(a) V_{GS} = 0V. (b) V_{GS} = -1V (c) V_{GS} = -4V.

Soln:

a) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$.

when V_{GS} = 0V. & $V_{DS} > |V_P|$

$I_D = I_{DSS}$ $\therefore$ $\boxed{I_D = 10mA}$

b) $V_{GS} = -1V$.

$I_D = 10\times10^{-3}\left[1 - \frac{(-1)}{(-4)}\right]^2 = 10\times10^{-3}(3/4)^2$

$\boxed{I_D = 5.625mA}$

c) $V_{GS} = -4V = V_P$.

$\boxed{I_D = 0A}$.

(A17a)

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For a JFET I_{DSS}=9mA and $V_{GS(off)}$=-8 $V_{(max)}$ determine drain current for V_{GS}= -4volts. **(04 Marks)** **Dec 2018-Jan 2019.**

Soln:-

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Given $V_{GS(off)} = -8$ volts $= V_P$.

and $V_{GS} = -4$ Volts,

$I_{DSS} = 9mA$

$$I_D = 9\times10^{-3}\left[1 - \frac{(-4)}{-8}\right]^2$$

$$= 9\times10^{-3}\left[1 - 1/2\right]^2$$

$$= 9\times10^{-3}\times(1/2)^2 = \frac{9}{4}\times10^{-3}$$

$$I_D = 2.25\times10^{-3}\ A$$

(a) $\boxed{I_D = 2.25mA}$

A18.

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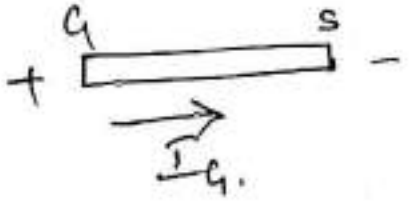
2. A JFET produces gate current of 2nA when gate is reverse biased with 8V. Determine the resistance between gate and source.

soln:- $I_G = 2nA$, $V_{GS} = 8V$.



using ohm's law

$$R_{GS} = \frac{V_{GS}}{I_G} = \frac{8}{2 \times 10^{-9}}$$

$$R_{GS} = 4 \times 10^9$$

$$\boxed{R_{GS} = 4000\ M\Omega}$$

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For a N-channel JFET if I_{DSS}=8mA and V_p= -5volts, calculate I_D at V_{GS}=-3volts and V_{GS} at I_D=3mA. **(05 Marks) June-July 2019.**

Soln:-

$V_p = -5\text{volts} = V_{GS(off)}$.

i. $I_D = ?$ at $V_{GS} = -3\text{volts}$,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$= 8\times10^{-3}\left[1 - \frac{(-3)}{(-5)}\right]^2$$

$$= 8\times10^{-3}\left[1 - 3/5\right]^2$$

$$= 8\times10^{-3}\left(2/5\right)^2$$

$$I_D = 8\times(2/5)^2\times10^{-3} = 1.28\times10^{-3}\ A$$

$$\boxed{I_D = 1.28\text{mA}}$$

ii. $V_{GS} = ?$ at $I_D = 3\text{mA}$.

$$V_{GS} = V_p\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= -5\left[1 - \sqrt{\frac{3\times10^{-3}}{8\times10^{-3}}}\right] = -5\left[1 - \sqrt{3/8}\right]$$

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$$V_{GS} = -5\left[1 - 0.6123\right]$$

$$\boxed{V_{GS} = -1.9381 \text{ volts}} \quad \underline{\simeq -1.94 \text{ volts}}$$

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For a N-channel JFET if I_{DSS}=9mA and V_p= -6volts, calculate I_D at V_{GS}=-4volts and V_{GS} at I_D=3mA. (05 Marks) Dec2019-Jan 2020.

Soln:-

i. $V_{GS} = -4$ volts $\quad I_D = ?$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$= 9\times10^{-3}\left[1 - \frac{(-4)}{(-6)}\right]^2$$

$$= 9\times10^{-3}\left[1 - 2/3\right]^2 = 9\times10^{-3}\left[1/3\right]^2$$

$$I_D = 1\times10^{-3}\ A$$

$$\boxed{I_D = 1mA}$$

ii. $V_{GS} = ?$ at $I_D = 3mA$.

$$V_{GS} = V_p\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= (-6)\left[1 - \sqrt{\frac{3\times10^{-3}}{9\times10^{-3}}}\right] = (-6)\left[1 - \sqrt{1/3}\right]$$

$$V_{GS} = (-6)\left[1 - 0.5773\right]$$

$$\boxed{V_{GS} = -2.535 \text{ volts}}$$

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Problem

The reverse gate voltage of JFET when changes from 4.4V to 4.2V, the drain current changes from 2.2mA to 2.6mA. Find out the value of transconductance.

Soln: transconductance $g_m = \left.\frac{\delta/p\ \delta}{i/p\ V}\right|$ for constant δ/p voltage.

$$g_m = \left.\frac{\text{change in } \delta/p \text{ current}}{\text{change in } i/p \text{ voltage}}\right| \text{ constant } \delta/p \text{ voltage.}$$

i.e $$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{Constant}}.$$

$$\Delta V_{GS} = 4.4 - 4.2 = 0.2V.$$

$$\Delta I_D = 2.2m - 2.6m = -0.4m.$$

$$g_m = \left|\frac{\Delta I_D}{\Delta V_{GS}}\right|$$

$$\boxed{g_m = \frac{0.4m}{0.2} = 2mV}$$

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A certain JFET has an I_{GSS} of -2nA for V_{GS} = -20V. Determine the input resistance. **(4 Marks) MQP-2**

Soln:-

$$I_{GSS} = -2nA$$

and $V_{GS} = -20V$

input Resistance of JFET

$$R_{in} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \frac{20}{2 \times 10^{-9}} = 10 \times 10^{+9}$$

$$R_{in} = 10,000 \times 10^{+6} \Omega$$

$$\boxed{R_{in} = 10,000 M\Omega}$$

Note:- Input Resistance (R_{in})

The input resistance R_{in} of JFET can be determined from a value of the gate reverse current I_{GSS} at a certain gate-to Source voltage.

i.e $\boxed{R_{in} = \left| \frac{V_{GS}}{I_{GSS}} \right| : \Omega}$.

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Explain the construction and operation of a p-channel JFET. (8 Marks)MQP-3

Soln:-

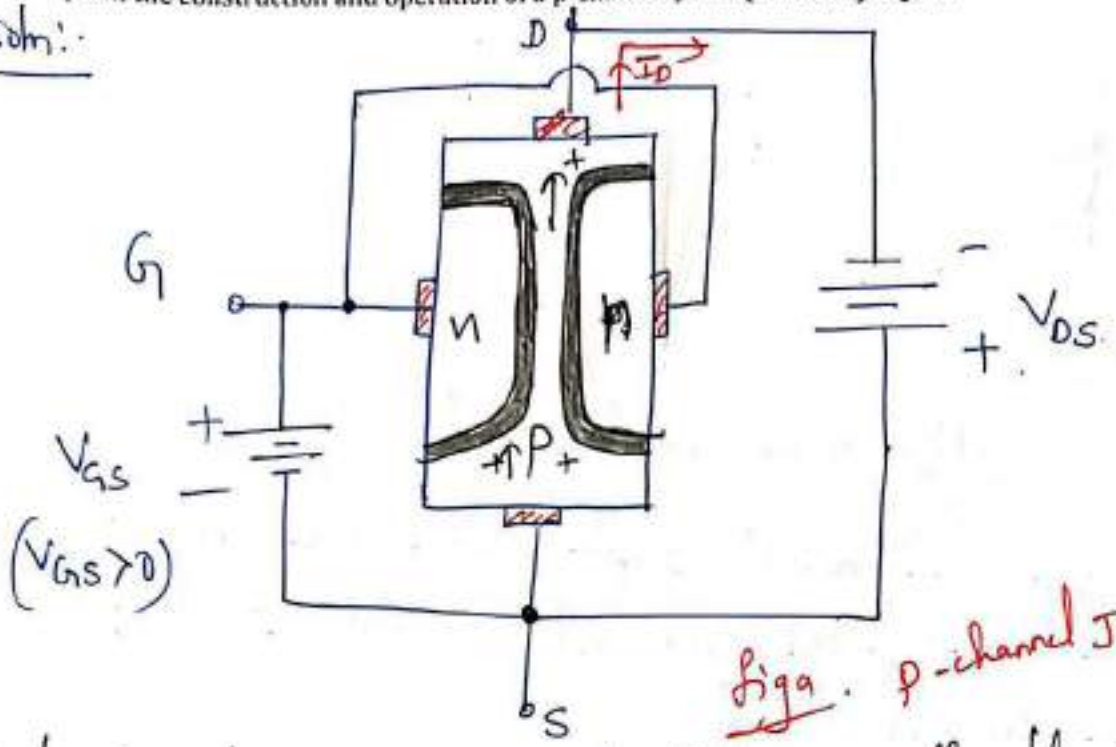

fig a. p-channel JFET.

* p-channel JFET is constructed in Exactly the same manner as the n-channel JFET but with reversal of the p- and n type materials as shown in fig a.
* all Current directions and voltage polarities are reversed.
* for $V_{GS}=0$, channel Width is maximum. By increasing positive gate to Source (V_{GS}) voltage, the channel width is reduced.

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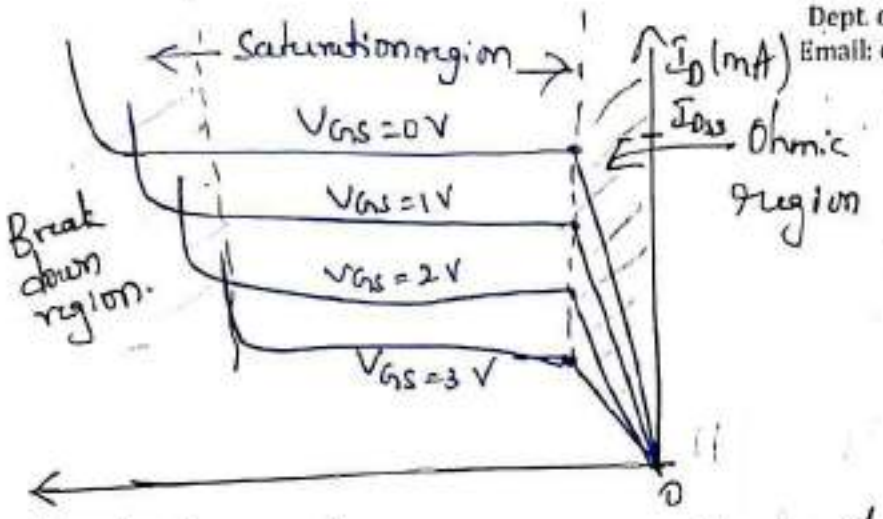

fig b. Drain characteristics of p-channel JFET.

* The curves are identical except that voltage V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

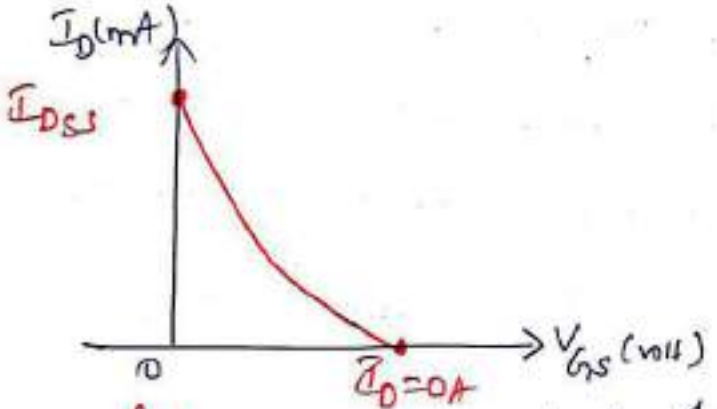

fig c. Transfer characteristics of p-channel JFET.

* fig c. shows that the transfer characteristics of p-channel JFET. it is identical to transfer characteristics of n-channel JFET except that polarities of V_{GS} and I_D are reversed.

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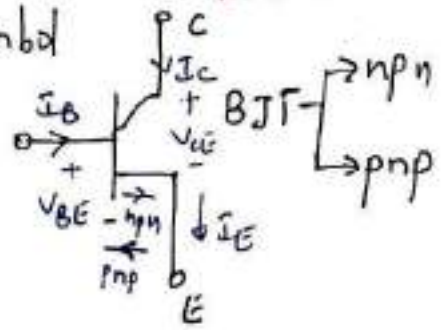
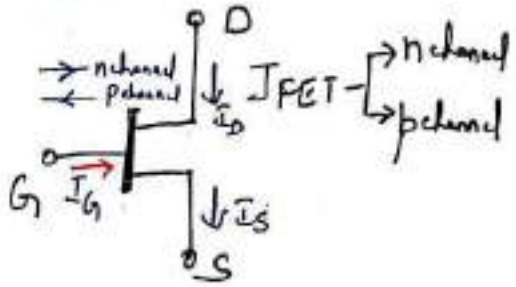
Comparision b/w BJT and FET

	BJT	FET
1.	Symbol 	
2.	input Current I_B Output Current I_C input voltage V_{BE} output voltage V_{CE}	i/p current is I_G o/p current is I_D i/p voltage is V_{GS} o/p voltage is V_{DS}
3.	$I_C = f^n(I_B) = \beta I_B$ (Controlled variable)	4. $I_D = f^n(V_{GS}) = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$ (Controlled variable)
5.	Current Controlled device (CCD)	5 voltage Controlled device (VCD)
6.	Bipolar charge carriers are both e^- and holes.	6. Unipolar device Charge carrier: either e^- (or) holes.
7.	$I_C \cong I_E$	7. $I_D = I_S$
8.	$V_{BE} = 0.7V$ (Si)	8. $I_G = 0A$. (B/c Gate junction is in RB)

Note: $I_G = 0A$, b/c gate terminal is at negative potential and n-channel is at positive potential which make p-n junction Reverse biased and $\therefore$ Current $I_G = 0A$.

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BJT	FET
9. Fanout is Good ↳ Maximum number of devices that can drive'.	9. Fanout - Bad.
10. Linear Amplifier $I_c = \beta I_B$	10. Non-Linear Amplifier. $I_D = I_{SS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$
11. Power consumption is high	11. power consumption is Low.
12. $(Z_i)_{BJT} < (Z_i)_{JFET}$	12. $(Z_i)_{JFET} > (Z_i)_{BJT}$
13. Bad thermal stability	13. Good thermal stability.
14. Sensitivity of BJT is Low	14. Sensitivity of JFET is high.
15. Noise Level ↑ (high)	15. Noise Level is Low (↓).
16. Size of BJT is large.	16. Size of JFET is Small. ∴ use it in IC Tehnology.
17. Gain ↑	17. Gain ↓.

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Problem1:

For JFET, determine I_D, if I_{DSS} = 12 mA, V_P = – 4 V and V_{GS} = – 1.

Sol. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= 12\times10^{-3}\left(1-\frac{(-1)}{(-4)}\right)^2$$

$$= 6.75 \text{ mA}$$

Problem2:

For JFET, determine V_P, if I_{DSS} = 8 mA, V_{GS} = – 2 V, and I_D = – 4 mA.

Sol. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$V_P = \frac{V_{GS}}{1-\sqrt{\frac{I_D}{I_{DSS}}}}$$

$$= \frac{-2}{1-\sqrt{\frac{4}{8}}}$$

$$= -6.828 \text{ V}$$

Problem 3:

For JFET, determine I_{DSS}, if I_D = 2 mA, V_{GS} = – 1 V and V_P = 5 V.

Sol. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$\therefore \quad I_{DSS} = \frac{I_D}{\left(1-\frac{V_{GS}}{V_P}\right)^2}$$

$$= \frac{2}{\left(1-\frac{(-1)}{(-5)}\right)^2}$$

$$= 3.125 \text{ mA}$$

JFET Parameters:

➢ ***List the important parameters of JFET.***

- The important parametres of JFET are as follows :
  - Input resistance
  - DC drain resistance
  - Dynamic (AC) Drain resistance (r_d)
  - Transconductance (g_m)
  - Amplification factor (μ)

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➢ Input resistance of JFET

- The input junction of JFET (gate - source junction) is reverse-biased and hence its input resistance is very high. The input resistance of JFET can be determined from a value of the gate reverse current, I_{GSS} at a certain gate-to-source voltage.

It is given by,

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

- Since I_{GSS} increases with temperature, input resistance decreases with temperature.

➢ ***Calculate the input resistance of JFET if I_{GSS} = - 2 nA when V_{GS} = - 15 V.***

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{15}{2\times10^{-9}}$$

$$= 7500\ M\Omega$$

➢ DC drain resistance

- The DC drain resistance is the resistance between drain and source terminals for the corresponding value of drain current, I_D and V_{DS}. It is denoted by R_D and mathematically given by,

$$R_D = \frac{V_{DS}}{I_D}$$

- Its value is few hundred kΩ.

➢ AC (Dynamic) drain resistance

- The drain resistance r_d is the a.c. resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain characteristic in the saturation region.
- It is given by,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ \text{constant}}$$

➢ JFET forward transconductance

- The forward transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant.
- The forward transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ \text{constant}}$$

- It is the slope of the transfer characteristic.
- The forward transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS (millisiemen) or mA/V.

➢ amplification factor of JFET

- The amplification factor, denoted by μ is defined as,

Amplification factor,

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D\ \text{constant}}$$

$$\therefore \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \boxed{\mu = r_d \times g_m}$$

- Since the parameter μ is the ratio of two similar quantities viz. ratio of two voltages; μ is unitless.

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Advantages of JFET

The advantages of FET are :

1. Extremely high input impedance, typically, of 100 meg-ohms.
2. Lower noise than BJT.
3. Easier to fabricate and are particularly suitable for ICs.
4. No offset voltage such as base-to-emitter voltage in BJT. This property is very important in the applications like switch, chopper, etc.
5. Immune to radiation.
6. Better thermal stability.
7. Low input capacitance.
8. Low frequency drift.
9. Draws very low power in the digital circuitry.

Applications of JFET

Applications of FET are :

- In general, like BJTs the FETs can be used in switch, digital and linear amplifier applications. Let us see specific applications of FET.
- Since JFET has high input impedance and low output impedance they are used as a buffer in measuring instruments.
- Because of low noise, they are used in RF amplifiers in FM tuners and in communication equipments.
- Since the input capacitance of FET is low, it is used in cascade amplifiers in measuring and test equipments.
- FETs are used in mixer circuits in FM and TV receivers, and communication equipments. Since use of FET reduces inter modulation distortion.
- Because of low frequency drift they are used in oscillators.
- FETs are also used in low frequency amplifiers.
- FETs are used in digital circuits.

Disadvantages of JFET

Disadvantages of FET are :

1. Poor performance at high frequency.
2. Small gain-bandwidth in comparison to the BJT.
3. Poor voltage gain.
4. Can be operated only in low power applications.

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MOSFET

[Metal oxide Semiconductor Field effect Transistors]

MOSFET → Active device.

ability to control the flow of electrons.

Eg:- BJT, FET, MOSFET.

Passive device:- ability to cannot control flow of electrons.

Eg:- Diode, Capacitor, Resistor, Transformer etc.

Classification of MOSFET

- Depletion type
  - n-channel
  - p-channel
- Enhancement type
  - n-channel
  - p-channel

Diff: n-channel [channel in their b/w Drain and Source].

[initial NO channel b/w Drain & Source].

Note:- construction of Depletion & Enhancement type mosfet both are same.

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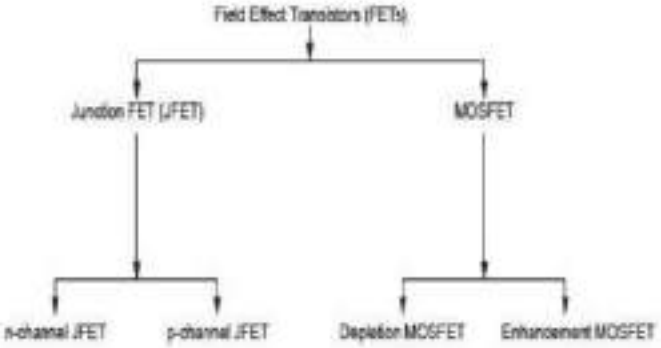
Introduction to MOSFET

- MOSFET (Metal Oxide Semiconductor Field Effect Transistor). It is a second category of field effect transistor.
- The MOSFETs, compared to BJTs, can be made very small and hence can be used to design high density VLSI circuits.
- The MOSFET differs from the JFET in that it has no p-n junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called IGFETs.



Types of MOSFET

- The two basic types of MOSFETs are :
  - Depletion (D) MOSFET and
  - Enhancement (E) MOSFET.
- The terms depletion and enhancement define their basic mode of operation.

Depletion Type MOSFET

a. Construction

- The Fig. shows the basic construction of n-channel depletion type MOSFET. Two highly doped n-regions are diffused into a lightly doped p-type substrate. These two highly doped n-regions represent source and drain.
- The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the Fig.
- The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, there is no direct electrical connection between the gate terminal and the channel of a MOSFET, increasing the input impedance of the device.

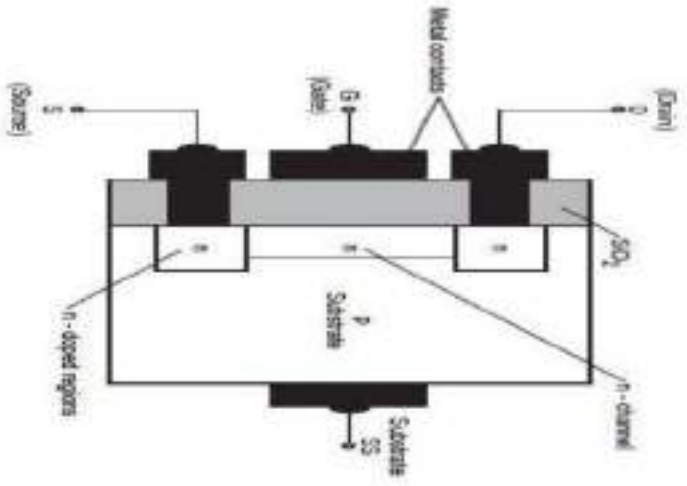


Fig. n channel Depletion type MOSFET

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b.Working of Depletion MOSFET

- On the application of drain to source voltage, V_{DS} and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0$ V.
- On application of negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, and attract holes from the p-type substrate. This initiates recombination of repelled electrons and attracted holes.
- Due to recombinations, n-channel is depleted of free electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of n-channel electrons. Thus, the level of drain current will reduce with increasing negative bias for V_{GS}.

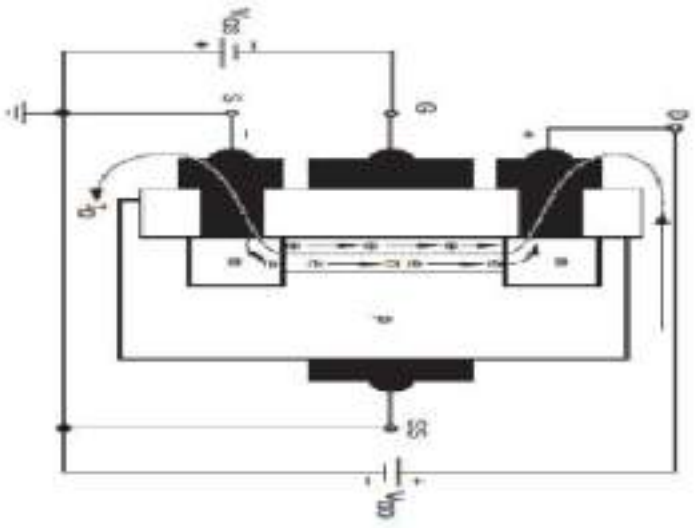

Fig. Working of Depletion Type MOSFET

c. Drain Characteristics of Depletion type MOSFET

- Fig. shows drain and transfer characteristics of n - channel depletion type MOSFET.

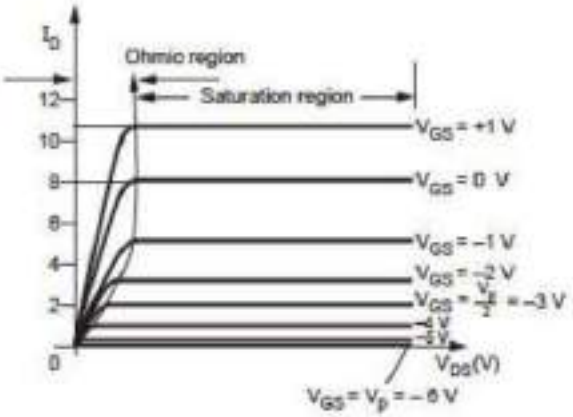

Fig. Drain characteristics for an n-channel depletion type MOSFET

Transfer Characteristics:

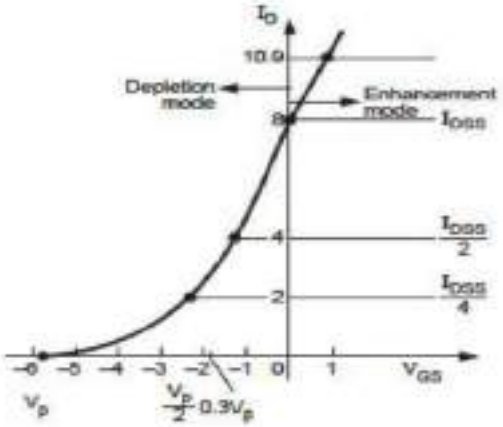

Fig. Transfer characteristics for an n-channel depletion type MOSFET

- The square law expression for the JFET also applies to the D-MOSFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$\approx I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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Problem:

For D-MOSFET, I_{DSS} = 8 mA and $V_{GS(off)}$ = – 4 V determine, a) Is this an n-channel or p-channel ?
b) I_D at V_{GS} = – 2 V c) I_D at V_{GS} = + 2 V

a) The device has a negative $V_{GS(off)}$, therefore it is an n-channel MOSFET.

b) $$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

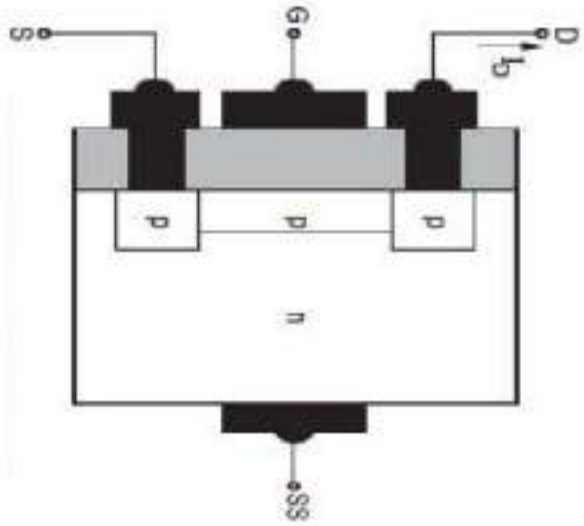
$$= 8\text{ mA}\left(1-\frac{(-2)}{(-4)}\right)^2 = 2\text{ mA}$$

c) $$I_D = 8\text{ mA}\left(1-\frac{(2)}{(-4)}\right)^2 = 18\text{ mA}$$

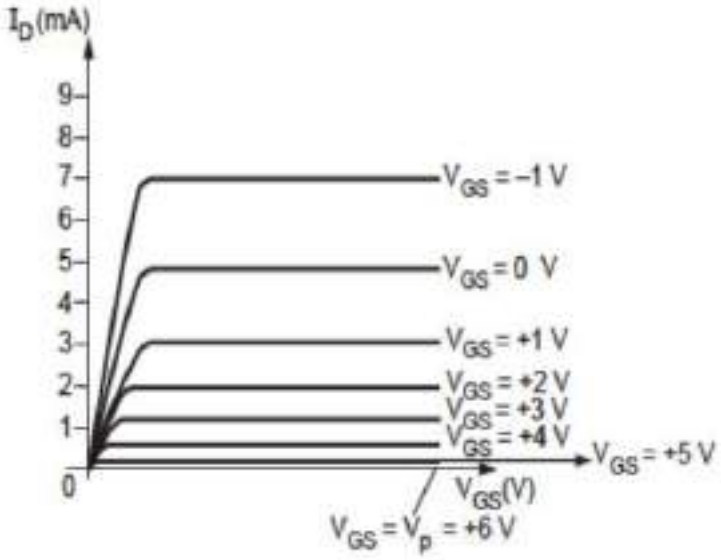
P-channel Depletion type MOSFET

a. Construction:

- The construction of the p-channel depletion type MOSFET is exactly opposite of that of n-channel depletion type MOSFET. Here, the substrate is of n-type, and regions and channel are of p type as shown in the Fig. (a).
- As shown in the Fig. (a) voltage polarities and current directions are reversed. The drain characteristics appear exactly as in Fig. (b) but V_{DS} with negative values, I_D in the opposite direction and V_{GS} having opposite polarities as shown in the Fig. (b).



(a) p-channel depletion type MOSFET



(b) Drain characteristics of p-channel depletion type MOSFET

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- Fig. (c) shows the transfer characteristics of p-channel depletion type MOSFET. In the p-channel depletion type MOSFET, the transfer characteristics is a mirror image about the I_D axis (Y axis) of the transfer characteristic of n-channel depletion type MOSFET, since the V_{GS} is positive in p-channel depletion region.

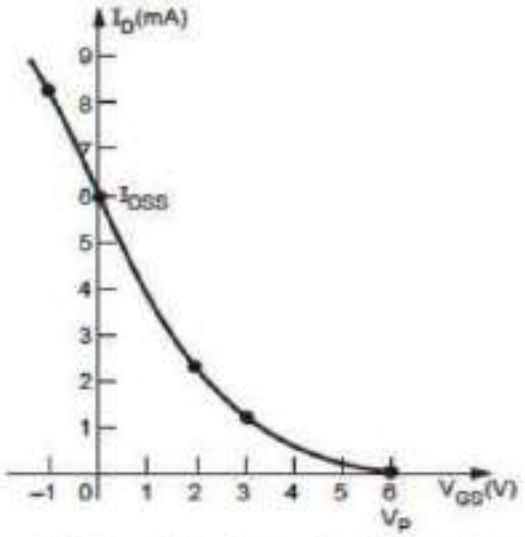

Fig. (c) Transfer characteristics of p-channel depletion type MOSFET

- Fig. shows graphic symbols for a n and p-channel depletion type MOSFET.

(a) Symbols for n-channel depletion type MOSFETs

(b) Symbols for p-channel depletion type MOSFETs

Fig. D-MOSFET symbols

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Topic 2. MOSFET N-channel Enhancement MOSFET.

Explain the operation of an enhancement MOSFET with neat circuit diagram. (06 Marks) Dec 2018-Jan 2019.

Explain the construction, working and characteristics of enhancement type MOSFET. (09 Marks) June-July 2019./ (09 Marks) Dec2019-Jan 2020/(8 Marks)MQP-3.

Soln:- Construction :-

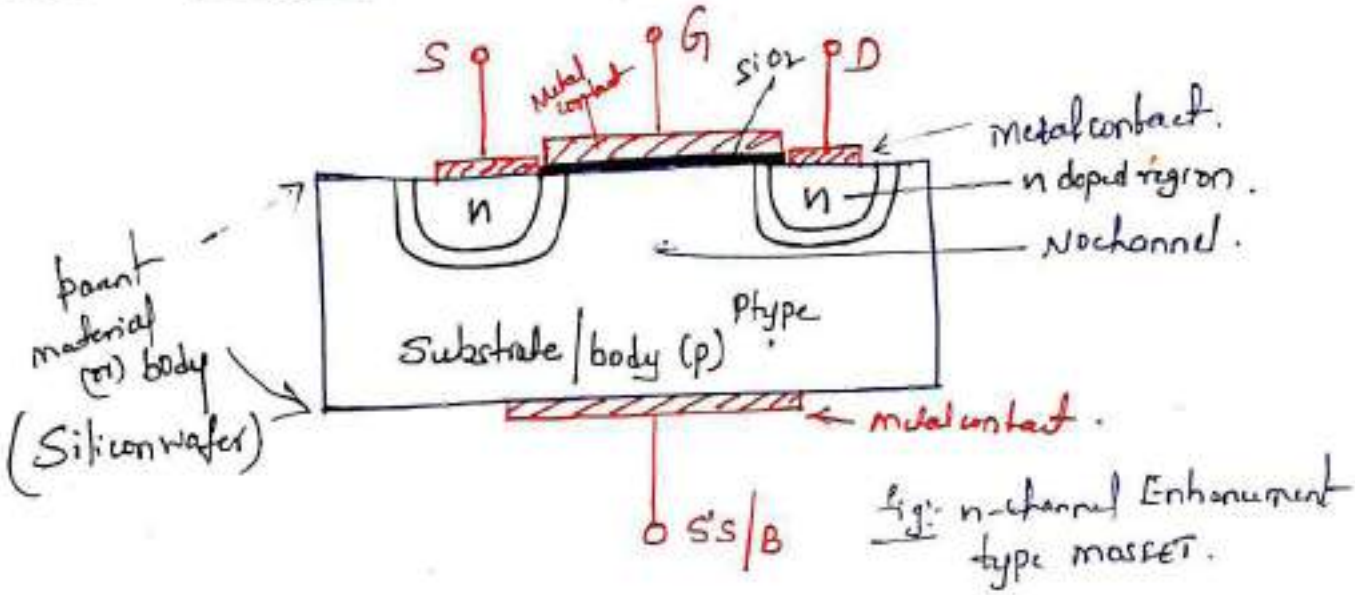

fig: n-channel Enhancement type MOSFET.

* parent material substrate / body in p-type.
* Two n-type wells are created. their in a junction blw two n type materials and p-type material is formed.
* One n-well act as Source and other one acts as Drain.
* the Substrate (or) body also having metal contact.
* Source and drain in n type and body in p-type.
* $SiO_2 \simeq 1000A^{\circ}$ very thin. also called Gate oxide.
* Obs:- No channel in blw Source & Drain.

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* Fig. shows the basic Construction of n-channel Enhancement type MOSFET.

* Two highly doped n-regions are diffused into a Lightly doped p-type Substrate. The Source and drain are taken out through metallic Contacts to n-doped regions as shown in the fig.

* The channel between two n-regions is absent in the Enhancement type MOSFET. The SiO_2 Layer is still present to isolate the gate metallic platform from the region between the drain and Source, but now it is simply Separated from a Section of the p-type material.

Working:

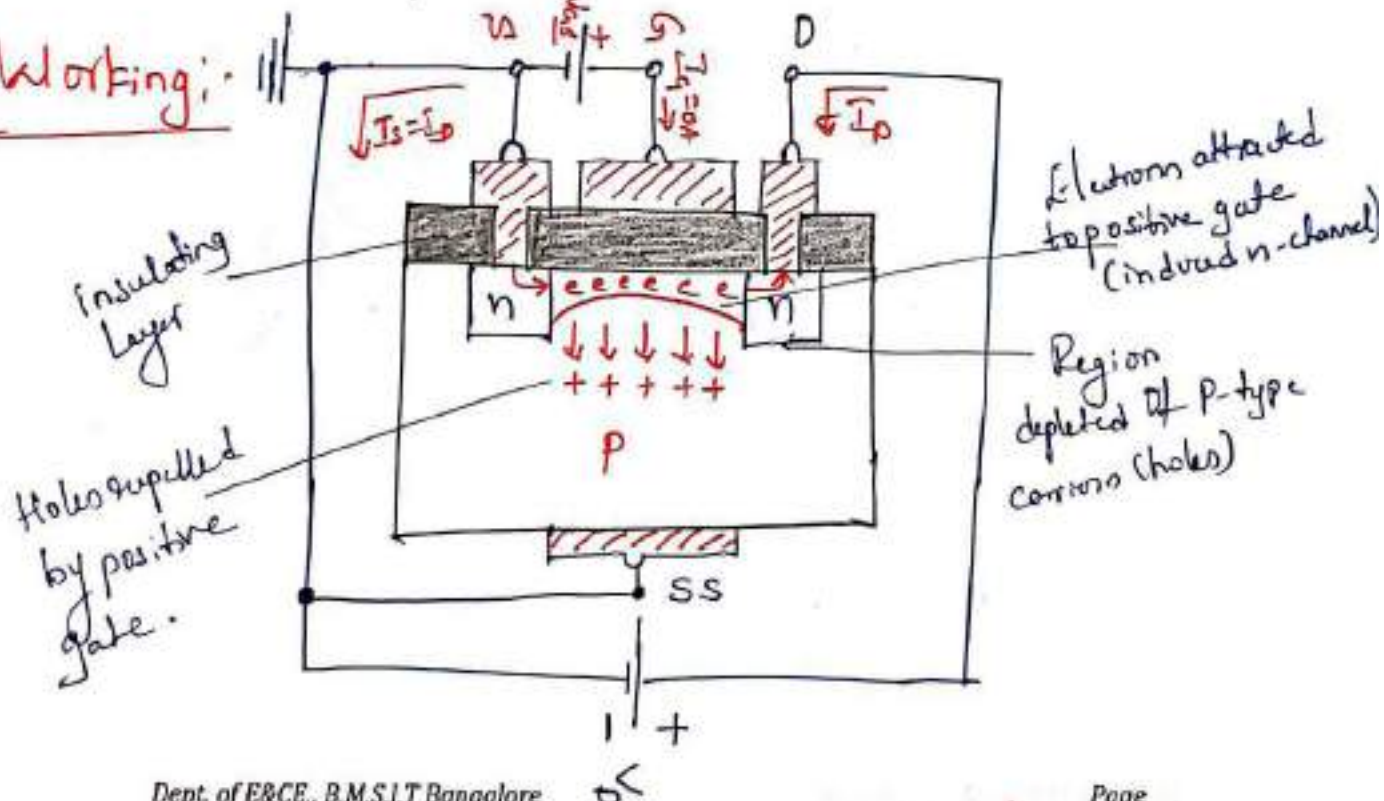

fig: Channel formation in the n-channel Enhancement type MOSFET.

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* On application of drain to Source voltage V_{DS} and keeping Gate to Source voltage Zero by directly connecting gate terminal to the Source terminal practically Zero Current Flows.
* If we increase Magnitude of V_{GS} in the positive direction the Concentration of electrons near the SiO_2 Surface increases. at a particular value of V_{GS} there is a Measurable Current flow between drain to Source. This value of V_{GS} is called threshold voltage denoted by V_t.
* A positive Gate voltage above a threshold value induces a channel and hence the drain Current.
* The conductivity of the channel is Enhanced by increasing the gate to Source voltage and thus pulling more electrons into the channel.
* Since the channel doesn't Exist with $V_{GS}=0V$ and "Enhanced" by the application of a positive gate to Source voltage, this type of MOSFET is called an Enhancement type MOSFET.

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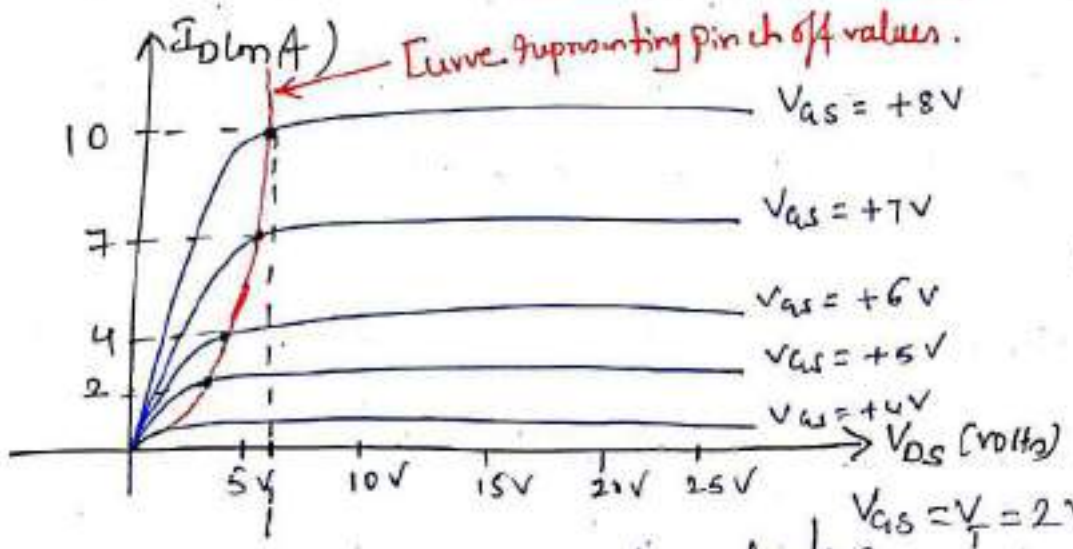
Drain Characteristics of an n-channel Enhancement MOSFET



$V_{GS} = V_T = 2V$.

Fig: Drain characteristics.

* as V_{GS} increasing beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain current.
However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level.
* The levelling off of I_D is due to a pinch-off process.

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Transfer characteristics :-

* Fig. shows the transfer characteristics of n-channel Enhancement type MOSFET.
* for $V_{GS} > V_T$, the relationship between drain current and V_{GS} is nonlinear and it is given as

$$I_D = K(V_{GS} - V_T)^2 \quad \leftarrow (1)$$

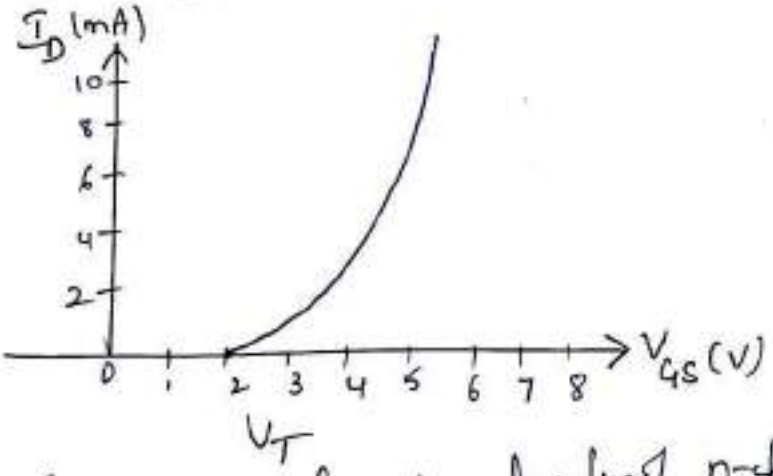

fig: Transfer characteristics of n-channel Enhancement type MOSFET.

* The term 'k' is constant that is a function of the construction of the device. The value of k can be determined from eq^n.

$$k = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_T]^2} \quad \leftarrow (2)$$

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For an EMOSFET, determine the value of I_D if $I_{D(on)}$=4mA, $V_{gs(on)}$=6volts, V_T=4volts and V_{gs}= 8volts. **(05 Marks) Dec2019-Jan 2020./(4Marks)MQP-1.**

Soln:-

$$K = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_T]^2}$$

$$= \frac{4 \times 10^{-3}}{[6-4]^2} = 1 \times 10^{-3} \, A/V^2.$$

$$\boxed{K = 1 \times 10^{-3} \, A/V^2}$$

$$I_D = K(V_{GS} - V_T)^2$$

$$= 1 \times 10^{-3} [8-4]^2$$

$$= 1 \times 10^{-3} (4)^2 = 16 \times 10^{-3} \, A.$$

$$\boxed{I_D = 16 \, mA}.$$

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P-channel Enhancement MOSFET

Explain the construction and working of P-channel enhancement type MOSFET. (8 Marks) MQP-1.

Construction:

- The construction of the p-channel enhancement type MOSFET is exactly opposite to that of n-channel enhancement type MOSFET. Here, the substrate is of n-type and regions are of p-type as shown in the Fig.

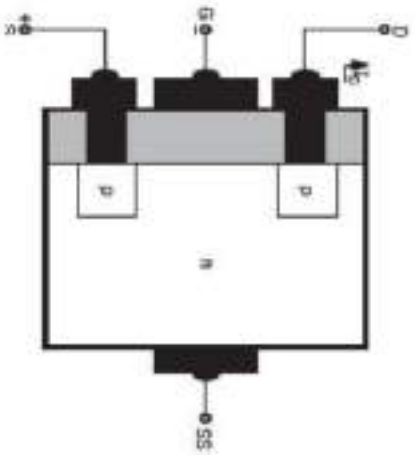

Fig. Construction of p-channel enhancement type MOSFET

- As shown in the Fig. voltage polarities and current directions are reversed. The drain characteristics appear exactly as in the Fig. but with V_{DS} with negative values, I_D in opposite direction and V_{GS} having opposite polarities as shown in the Fig.

Drain Characteristics:

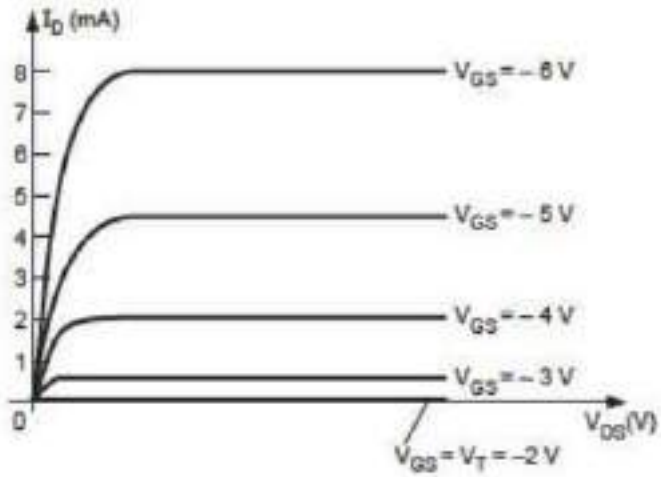

Fig. Drain characteristics of p-channel enhancement MOSFET

Transfer Characteristics:

- Fig. shows the transfer characteristics of p-channel enhancement type MOSFET. In the p-channel enhancement type MOSFET, the transfer characteristic is a mirror image about the I_D axis (y axis) of the transfer characteristics of n-channel depletion type MOSFET, since the V_{GS} is negative.

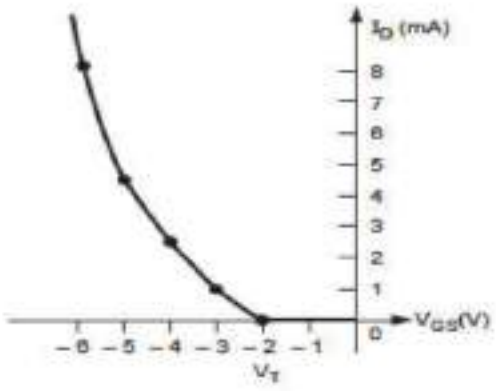

Fig. Transfer characteristics of p-channel enhancement type MOSFET

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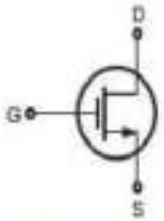
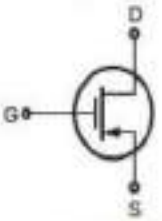
symbols of E-MOSFET.

- Fig. shows graphic symbols for n and p-channel enhancement type MOSFET.



Simplified symbol

(a) Symbols for n-channel enhancement type MOSFETs



Simplified symbol

(b) Symbols for p-channel enhancement type MOSFETs

Problems:

Ex. *For a depletion type MOSFET, determine I_D if $V_{GS} = -1$ V, $V_P = -4$ V and $I_{DSS} = 16$ mA.*

Sol. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= 16\left(1-\frac{(-1)}{(-4)}\right)^2$$

$$= \mathbf{9\ mA}$$

Ex. *For a depletion type MOSFET, determine V_P, if $V_{GS} = -1$ V, $I_D = 8$ mA and $I_{DSS} = 12$ mA.*

Sol. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$8 = 12\left(1-\frac{(-1)}{V_P}\right)^2$$

$$V_P = \frac{1}{\sqrt{\frac{8}{12}}-1}$$

$$= \mathbf{-5.45\ V}$$

Ex. *For a depletion type MOSFET, determine value of I_{DSS}, if $I_D = 10$ mA, $V_{GS} = -2$, $V_P = -4$ V.*

Sol. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$I_{DSS} = \frac{I_D}{\left(1-\frac{V_{GS}}{V_P}\right)^2} = \frac{10\text{ mA}}{\left(1-\frac{(-2)}{(-4)}\right)^2}$$

$$= \mathbf{14.14\ mA}$$

Ex. *For E-MOSFET, determine value of I_D, if $I_{D(ON)} = 4$ mA, $V_{GS(ON)} = 6$ V, $V_T = 4$ V and $V_{GS} = 8$ V.*

Sol. :

$$K = \frac{I_{D(ON)}}{\left(V_{GS(ON)}-V_T\right)^2}$$

$$= \frac{4\times10^{-3}}{(6-4)^2} = 1\times10^{-3}\ A/V^2$$

$$I_D = K(V_{GS}-V_T)^2$$

$$= 1\times10^{-3}(8-4)^2 = \mathbf{16\ mA}$$

Ex. *For E-MOSFET, determine value of V_T, if $K = 1$ mA/V^2, $I_{D(ON)} = 4$ mA, $V_{GS(ON)} = 5$ V.*

Sol. :

$$K = \frac{I_{D(ON)}}{\left(V_{GS(ON)}-V_T\right)^2}$$

$$V_T = V_{GS(ON)} - \sqrt{\frac{I_{D(ON)}}{K}} = 5-\sqrt{\frac{4}{1}} = \mathbf{3\ V}$$

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Advantages of MOSFET over JFET

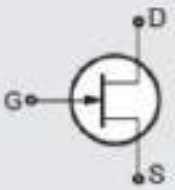
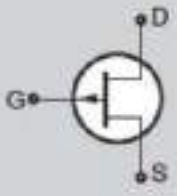
➢ ***State the advantages of MOSFET over JFET ?***

The advantages of MOSFET over JFET are :

- Input resistance of MOSFET is higher than JFET.
- JFET can be operated in only depletion mode, however, MOSFET can be operated in enhanced mode as well as depletion mode.
- It can operate with positive as well as negative gate voltages.

Comparison between JFETs and MOSFETs

➢ ***Compare n - channel JFET and p - channel JFET.***

Sr. No.	n-channel JFET	p-channel JFET
1.	Symbol 	Symbol 
2.	Electrons are the current carriers.	Holes are the current carriers.
3.	Mobility of electrons is large in n-channel JFET.	Mobility of holes is poor in p-channel JFET.
4.	Input noise is less.	Input noise is more.
5.	Large transconductance.	Less transconductance.

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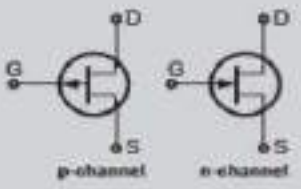
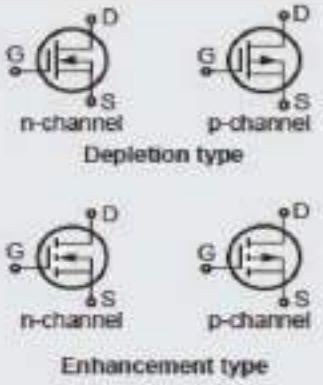
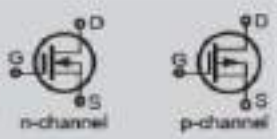
➢ ***Compare JFET and MOSFET.***

Sr. No.	Parameter	JFET	MOSFET
1.	Types	a) n-channel b) p-channel	A) n-channel depletion type MOSFET B) p-channel depletion type MOSFET C) n-channel enhancement type MOSFET D) p-channel enhancement type MOSFET
2.	Symbols		
3.	Operation mode	Operated in depletion mode.	Operated in depletion and enhancement mode.
4.	Input impedance	High (> 10 MHz)	Very high (> 10,000 MΩ)
5.	Gate	Gate is not insulated from channel.	Gate is insulated from channel by a layer of SiO_2.
6.	Channel	Channel exists permanently .	Channel exists permanently in depletion type MOSFET, but not in enhancement type MOSFET.

➢ ***Compare D - MOSFET and E - MOSFET.***

Sr. No	Parameter	Depletion type	Enhancement type
1.	Symbols		
2.	Channel	Exists permanently.	Channel is physically absent. It is induced after application of positive gate voltage above the threshold value for n-channel enhancement type MOSFET and negative gate voltage above threshold value for p-channel enhancement type MOSFET.
3.	Operation	Can be operated in depletion mode as well as enhance mode.	Can only be operated in enhance mode.
4.	Current flow	Drain current flows on application of drain to source voltage, at $V_{GS} = 0$.	Practically no current flows on application of drain to source, at $V_{GS} = 0$. Current flows only when V_{GS} is above threshold level.

"Tell me and I Forget, Show me and I remember, Let me do and I Understand"

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Complementary Metal oxide Semiconductor.

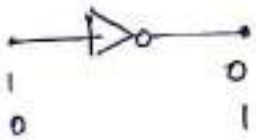
Topic 3. CMOS

Explain CMOS as an inverter with neat circuit diagram. Give its equivalent circuit and its advantages. (08 Marks) Dec 2018-Jan 2019.

With a neat circuit diagram explain the working of CMOS inverter. (06 Marks) June-July 2019./ (06 Marks) Dec2019-Jan 2020./ (6 Marks)MQP-1./ (7 Marks)MQP-2/(6 Marks)MQP-3

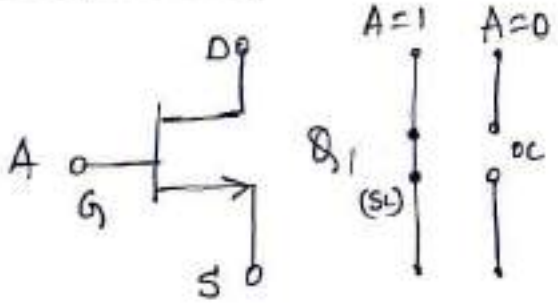
Soln:- Fundamentals:-

* Inverter



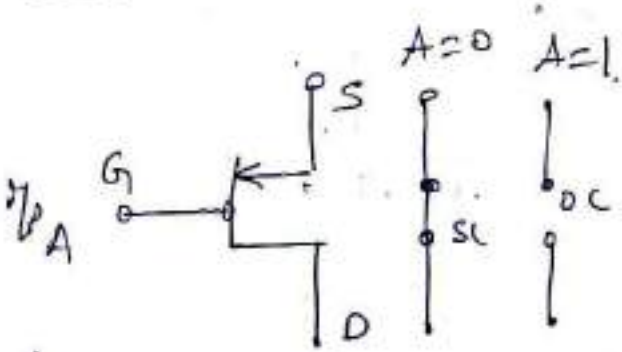
* N.E.T in NMOS $I_D[D \rightarrow S]$
and pmos $I_D[S \rightarrow D]$.

NMOS operation:-



if A = 1 then transistor behaves as closed switch.

PMOS



if A = 0, then transistor behaves as closed switch.

CMOS INVERTER:-

* CMOS is the Complementary MOS wherein two enhancement MOSFETs one N-type (NMOS) and other p-type (pmos), are connected as a complementary pair.

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* The two gates are connected to form the input terminal and the two Drains are connected to form the output terminal as shown in fig.

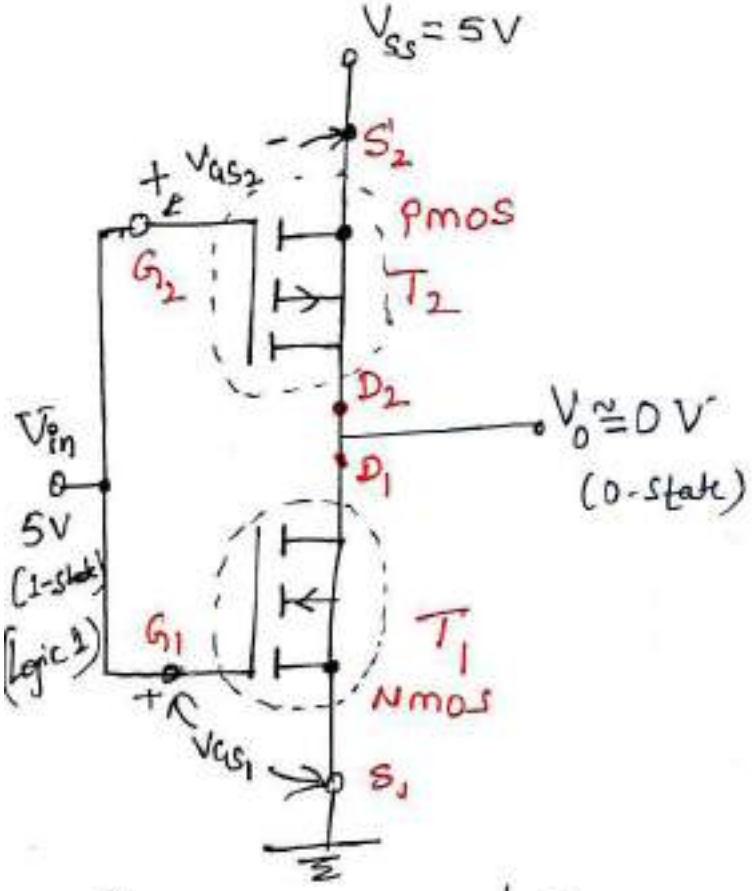

fig a. Cmos inverter

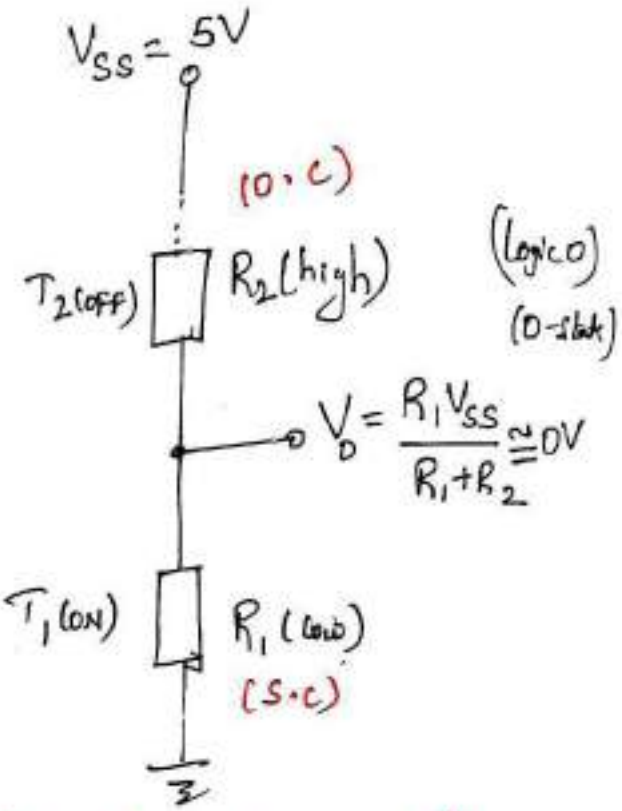

fig b. Equivalent circuit for $V_i = 5V$, state 1 (logic 1)

fig:- Emos Circuit.

Table:-

input (V_i)	T_1	T_2	output (V_0)
0V (logic 0)	OFF (o.c)	ON (s.c)	5V (logic 1)
5V (logic 1)	ON (s.c)	OFF (o.c)	0V (logic 0)

B_2

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Operation :-

Case i. Input $V_i = 5V$ (Logic 1).

$V_{GS_2} = 5 - 5 = 0$ Volts

T_2 is nonconducting, (OFF) $\rightarrow$ (oc), drawn only leakage current offers high resistance (R_2).

T_1 is conducting (ON) $\rightarrow$ (sc); offer very low resistance (R_1).

output $\boxed{V_0 \cong 0 \text{ volts}}$ (Logic-0).

i.e $V_0 = \frac{R_1}{(R_1+R_2)} \cdot V_{SS} \cong 0$ volts

Case ii. input $V_i = 0$ Volts $\Rightarrow$ Logic-0.

$V_{GS_2} = -5V$, T_2 conducting (Low resistance)

$V_{GS_1} = 0V$; T_1 non conducting (high resistance)

output $\boxed{V_0 \cong 5V} \Rightarrow$ (Logic-1)

i.e the Circuit act as an inverter; Logic-1 input produces Logic-0 output and Vice-versa.

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Obs:-

i. In the circuit only one transistor is turned 'ON' in any of the output states

ii. As the transistors are connected in series, no current is drawn from the battery source in either of the two states. Current is drawn from battery only during state transitions [i.e switch from logic 0 to logic 1 vice-versa].

iii. ∴ Cmos circuits, ∴ draws extremely low power from the battery source and so their energy consumption is very small. This is the major attraction why cmos is used in digital application.

Adv.

Advantages of cmos Circuit

i. The drain current is very low and flows mainly during transition from one state to the other (ON/OFF).

ii. The power drawn in steady state is extremly small.

iii. cmos ckts consumes less power.

iv. Can be operated at high voltages to improve noise immunity.

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Silicon Controlled Rectifier (SCR)

* SCR is a 4 Layer, three junction p-n-p-n Semiconductor switching device.
* SCR is a "Semiconductor switching device" used as a "Controlled Switch for rectification.

Construction:-

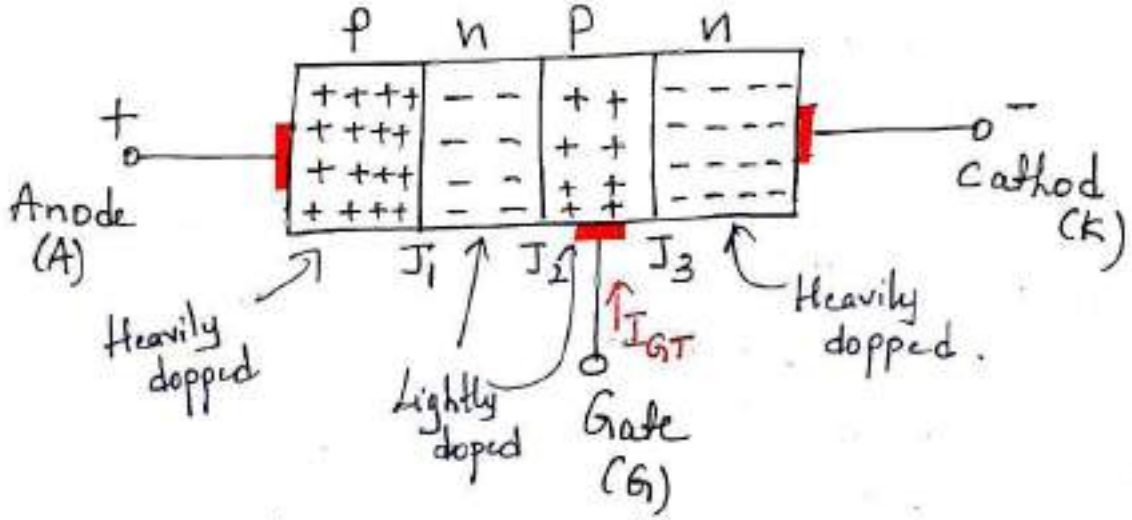

fig a: Construction of SCR.

* The fig b. shows the symbol of SCR.

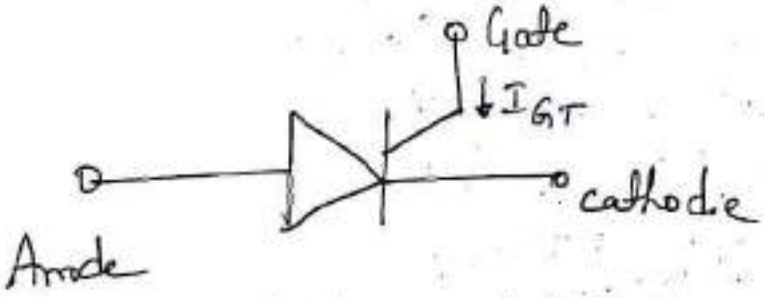

fig b. Symbol of SCR.

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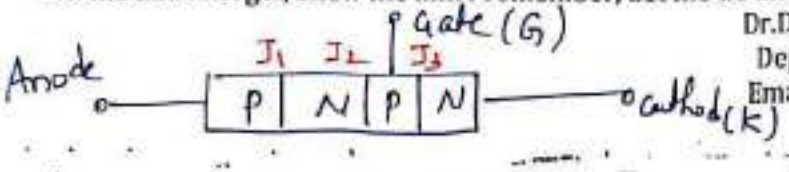
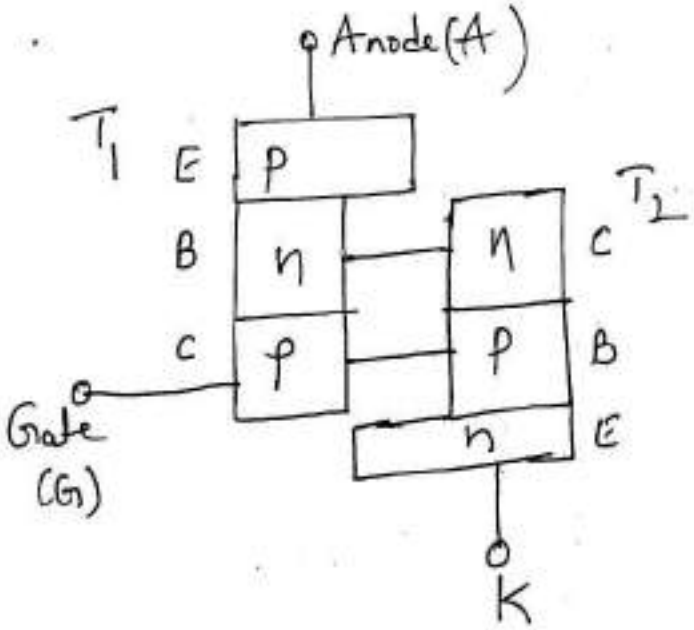


* SCR is a four Layer p-n-p-n device where p and n-Layers are alternately arranged. The outer layers are heavily doped while inner layers are lightly doped.
* There are three p-n junctions called J_1, J_2 and J_3.
* The outer 'p' Layer is called anode and outer 'n' layer is called cathode. Middle p layer is called gate.

Equivalent Circuit:-

SCR is a two diodes connected back to back (or) two transistors connected back to back.



T_1 – pnp
T_2 – npn
} Transistors

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Working of SCR :-

Topic 4. SCR

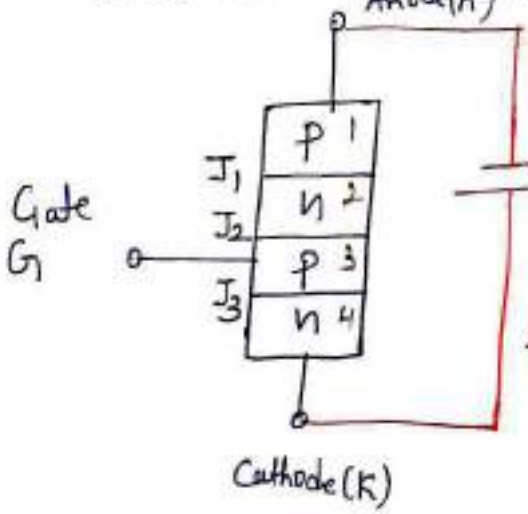
Explain V-I characteristics of SCR (06 Marks) Dec 2018-Jan 2019./ (6 Marks)MQP-2/(6 Marks)MQP-3

Soln:- SCR has three basic modes of operation.

i. Reverse blocking mode.
ii. Forward blocking (off-state) mode.
iii. forward condution (ON-state) mode.

i. Reverse blocking Mode.

* In Reverse blocking mode cathode is made more positive than anode. i.e $V_{anode} < V_{cathode}$.



* Junctions J_1 and $J_3 \Rightarrow$ R·B and $J_2 \Rightarrow$ F·B.

* Since J_1 & J_3 are R·B ∴ No Current flow in the ckt.

* if we increase the External bias voltage greater than the Reverse breakdown voltage (V_{BR}), Avalanch Breakdown it occurs.

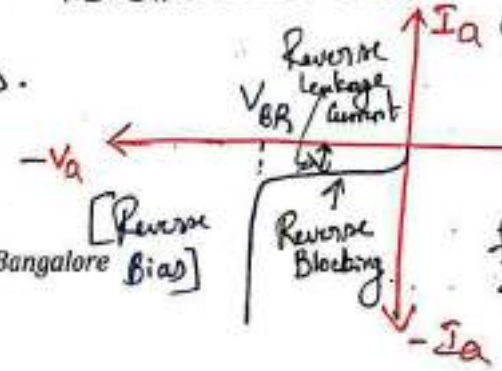


fig a. Reverse blocking Mode Ia Vs Va.

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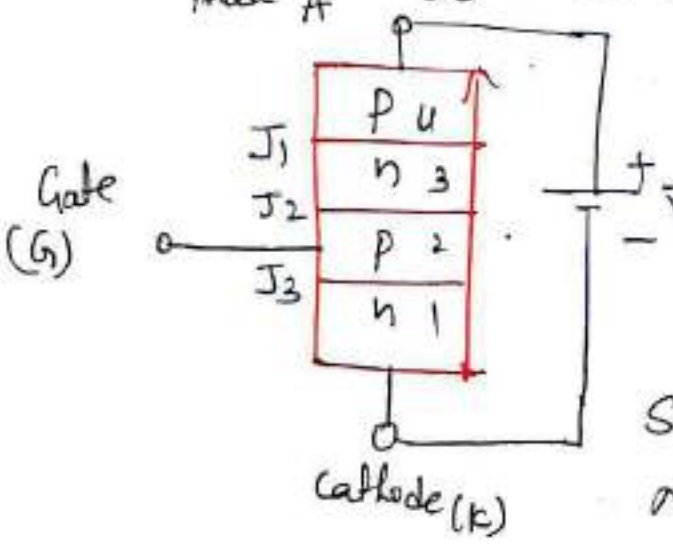
ii) Forward Blocking Mode:- In this mode of operation

* Anode is make positive than the cathode.

i.e $V_{anode} > V_{cathode}$.

but $< V_{BO}$ (break over voltage).



* Junctions J_1 and J_3 are F.B.

* Junction J_2 is R.B.

Since Junction J_2 is R.B NO Current will flows in the circuit

∴ circuit acts as a open switch.

* When Anode voltage is keep on increasing in comparision with cathode, at one particular voltage their will be a Breakdown occurs at Junction J_2, results large amount of Current will starts flow.

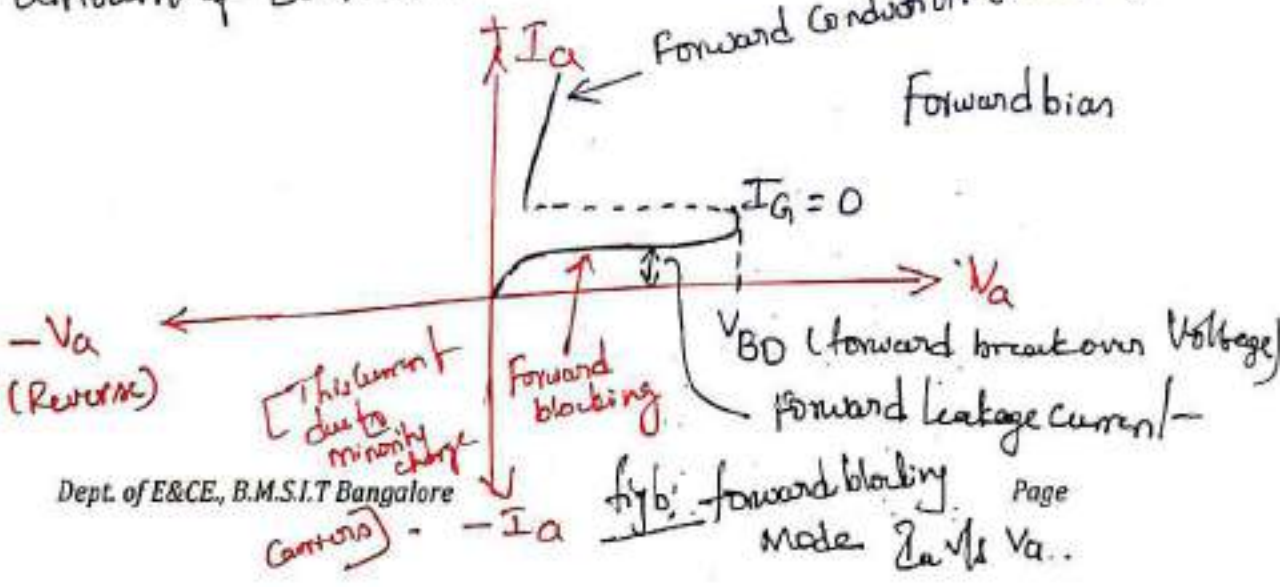


fig: forward blocking mode Ia Vs Va.

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iii. Forward Conduction Mode:-

In this Mode $V_{anode} > V_{cathode}$.

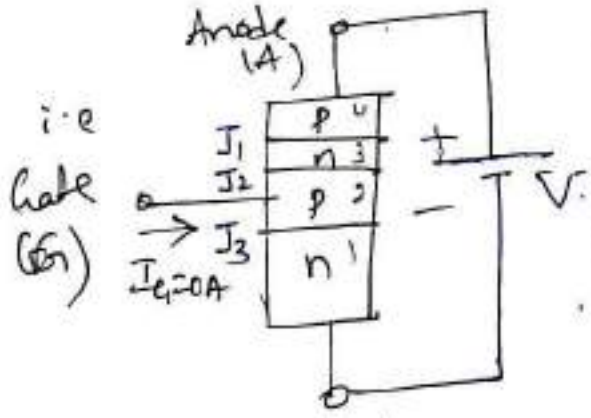
& $> V_{BO}$.

(or)

By applying Gate pulse.

* To use SCR as an ON switch (i.e S.C). there are two ways.

Method 1:- By increasing anode voltage more than the forward Breakover voltage Result's at Junction J_2 Break down occurs ∴ large Current will starts flowing in the Circuit.



$V_{Anode} > V_{cathode}$ and $> V_{BO}$

i.e

$\Rightarrow$ J_1 & J_3 are F.B

if $V_A > V_{BO}$ and ∧ Break down occurs at Junction J_2 ∴ Current starts flowing.

and at this Method $I_G = 0A$.

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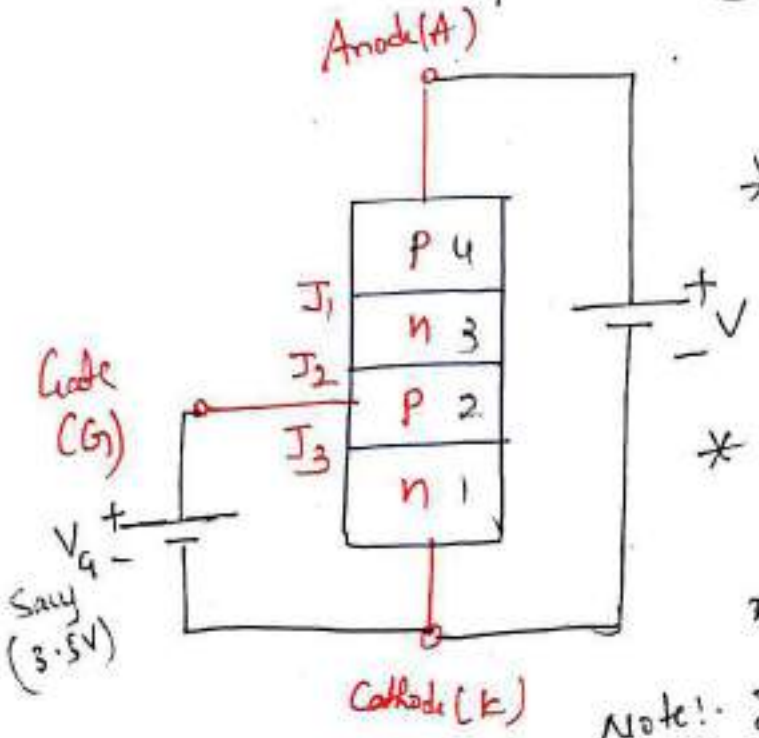
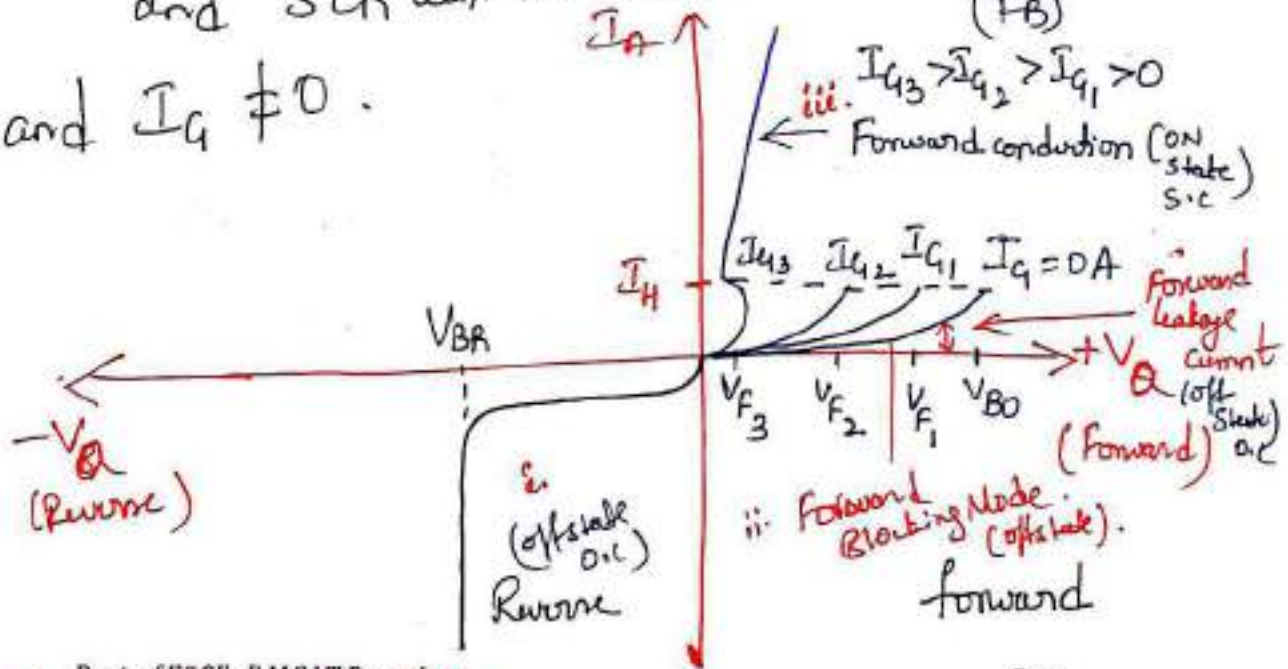
Method 2:- By applying +ve Gate pulse. (or) applying potential at Gate terminal.



* In this Mode of operation Junction J_1 and J_3 acts as F.B.
* due to external +ve Gate pulse Junction J_2 will be under F.B condition.

Note:- In forward conduction Mode all the Junctions J_1, J_2 and J_3 will be in forward -biased Mode ∴ Current Flows in a Circuit easily and SCR acts as Short Circuit (or) closed Switch. and $I_G \neq 0$.



$V_{F_3} < V_{F_2} < V_{F_1} < V_{BO}$.

fig:- I-V characteristics of SCR.

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Defn

ii. Forward Break over voltage V_F @ V_{BO} :-

* Forward Break-over Voltage V_F @ V_{BO} is the voltage at which for a given I_G, the SCR enters into conduction mode.
* The forward Break-over voltage reduces as I_G increases.

i.e $I_{G3} > I_{G2} > I_{G1} > 0$.

$\Rightarrow V_{F3} < V_{F2} < V_{F1} < V_{BO}$.

iii. Holding Current (I_H).

Holding current I_H is the value of the current below which SCR switches from Conduction state (ON state) to forward blocking region/state (off-state).

iii. Reverse breakdown voltage (V_{BR}).

It is the reverse voltage (Anode-negative and cathode-positive) above which the reverse breakdown occurs, breaking J_1 and J_3 Junctions.

G

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Note:-

i. Reverse blocking Mode. [SCR - off]

J_1 J_3 ⇒ R.B
J_2 ⇒ F.B

} No Current flows in ckt. SCR acts as a O.C (open ckt).

ii. forward blocking Mode [SCR - offstate]

J_1 J_3 ⇒ F.B
J_2 ⇒ R.B

} Small leakage current due to Minority charge carriers

SCR - offstate acts as a open ckt (O.C).

iii. forward condition Mode:- (SCR ON state SC).

J_1, J_2, J_3 ⇒ F.B.

Current flows in ckt. since SCR acts as shortckt.

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What is SCR ? Explain the working of SCR using two transistor model. **(06 Marks) June-July 2019./ (06 Marks) Dec2019-Jan 2020./ (8Marks)MQP-1./ (6 Marks)MQP-2/(6 Marks)MQP-3**

Sol^n:- "SCR is a four layered, three junction, three terminal Silicon Semiconductor Controlled Rectifier".

* The two transistor Model of SCR is shown in the fig.

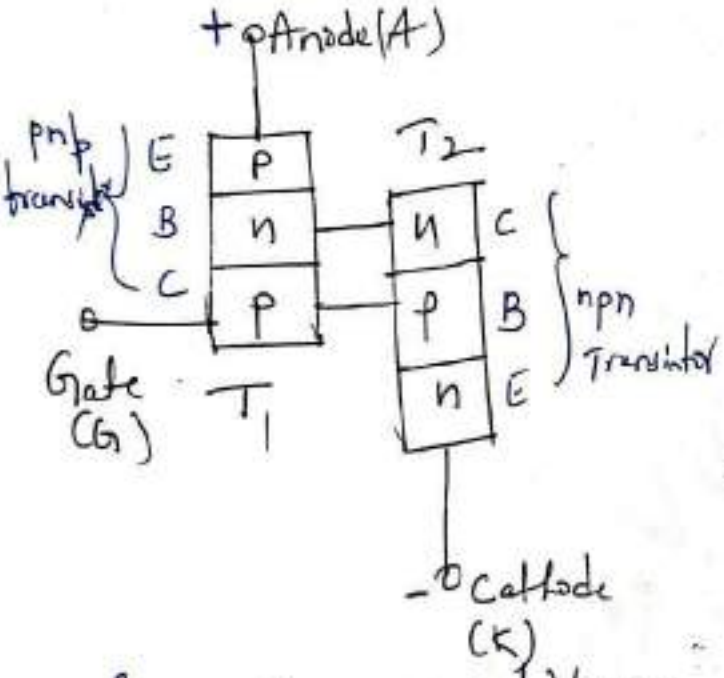

fig a: From Sectional View.

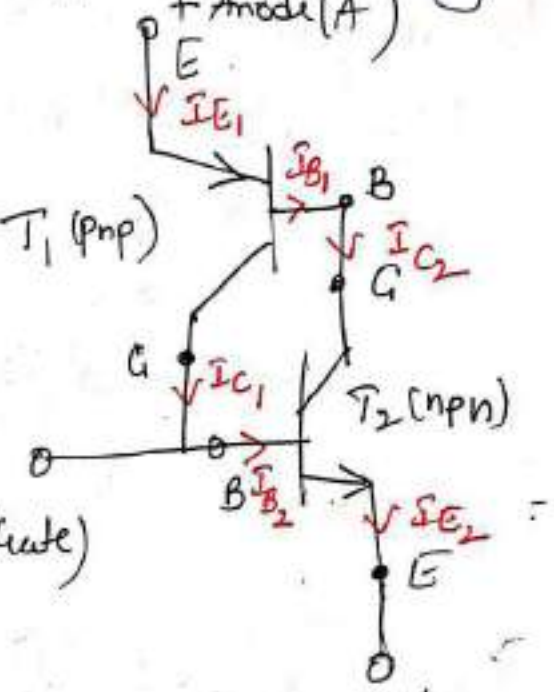

fig b:- Equivalent ckt

fig:- Two transistor Model.

* The base of pnp is connected to the collector of npn transistor. and the collector of pnp is connected to the base of npn. While the gate is connected to the base of npn (or) collector of pnp transistor.

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* The Corresponding two-transistor Equivalent circuit is shown in fig b. observe that the connections are consistent with fig a.

* The Collector Current of T_1 becomes base current of T_2 and collector current of T_2 becomes base current of T_1.

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What is commutation in SCR? Explain two types of communication. **(05 Marks) June-July 2019.**

Soln:- **Commutation:-** SCR is turned ON by applying gate pulse. But when SCR conducts, the gate pulse has NO control on its conduction. Hence it can not be turned off by removing gate pulse. They external circuit is required to turn off SCR.

The Mechanism of turning-off the SCR is called Commutation.

Types:-

i. Natural Commutation.

ii. Forced Commutation.

i. Natural Commutation:-

* The natural Commutation is also called Line commutation, because it uses Supply Line voltage for turning off the SCR.
* The Supply voltage Naturally pass through zero due to which current through SCR becomes zero at the instant when Line voltage becomes zero.

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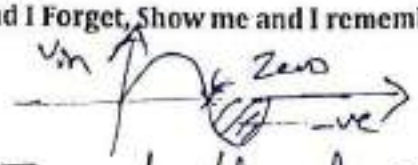

* As the Current through SCR becomes Zero, the SCR turns off.
* After passing through Zero, the a.c voltage becomes negative which appears across the SCR and it does not conduct.
* Thus natural Commutation takes place without any external Components hence it is called natural Commutation.
* for the Natural Commutation, Supply voltage must be a.c it cannot be used for d.c voltage.

ii). Forced Commutation of SCR :-

* The forced Commutation is used when the supply is d.c.
* A Commutation requires External Circuit which is Connected across SCR. is called forced Commutation.
* The Current through SCR is forced to become Zero by passing a current in opposite direction using an External Circuit.
* fig. shows One of the turn-off circuits used for forced Commutation.

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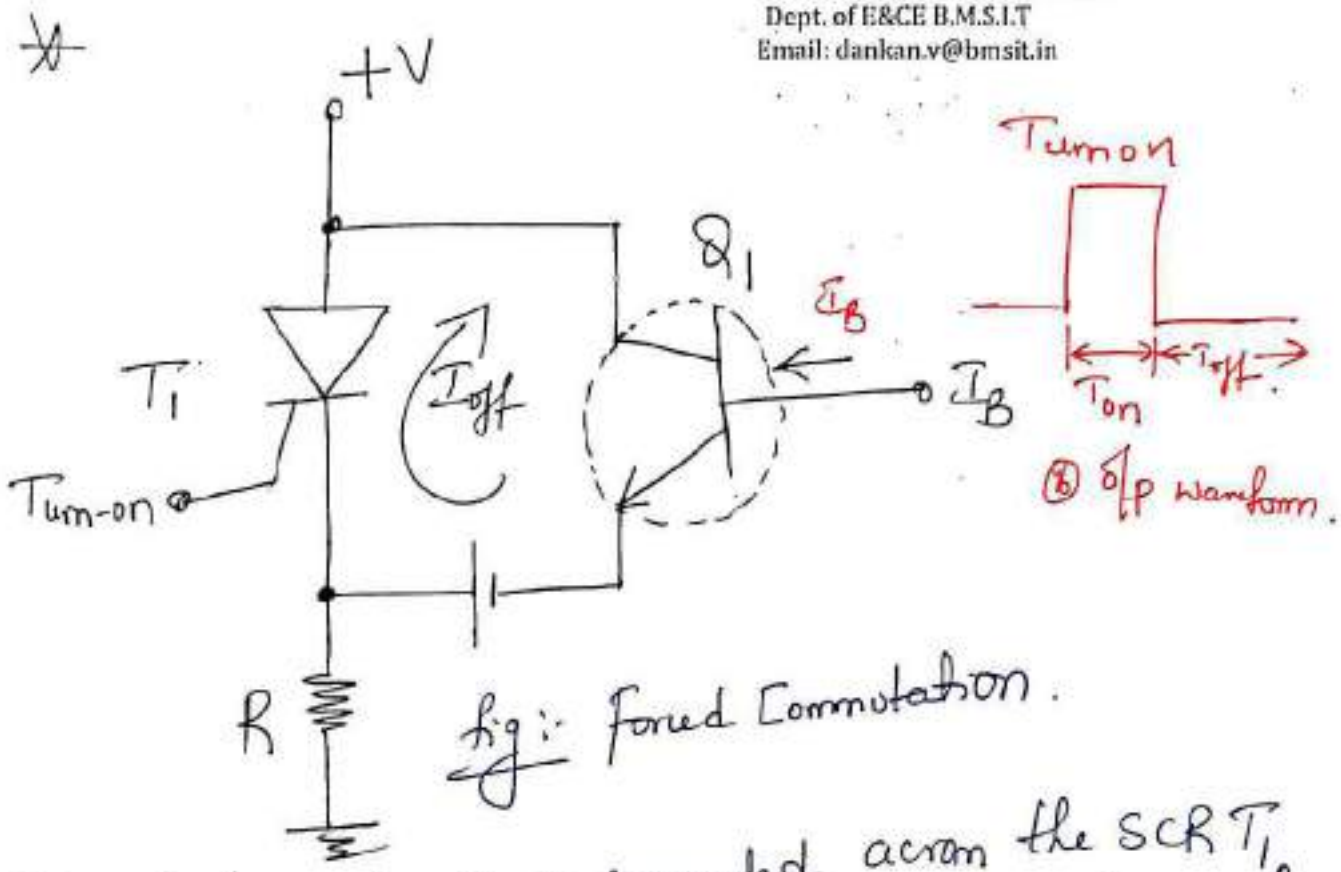

fig:- Forced Commutation.

* A transistor Q_1 is connected across the SCR T_1. When SCR is conducting I_B is zero and Q_1 is off.
* To turn-off SCR, a positive pulse is applied to base of Q_1, which drives Q_1 in saturation and circulates high current I_{off}, in opposite direction to the conduction current of SCR.
* This drops SCR total current below the holding current and the SCR turns-off.
* turn-off time of an SCR is typically 5-30 μsec.

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Comparison between Natural and Forced Commutation:

Sr. No.	Natural commutation	Forced commutation
1.	No external commutation components are required.	External commutation components are required.
2.	Requires AC voltage at the input.	Works on DC voltages at the input.
3.	Used in controlled rectifiers, AC voltage controllers etc.	Used in choppers, inverters etc.
4.	No power loss takes place during commutation.	Power loss takes place in commutating components.
5.	SCR turns-off due to negative supply voltage.	SCR can be turned-off due to voltage and current both.
6.	Cost of the commutation circuit is nil.	Cost of the commutation circuit is significant.

==========

Merits or Advantages of SCR

merits of SCR.

1. Very small amount of gate drive is required.
2. SCRs with high voltage and current ratings are available.
3. On state losses of SCR are less.
4. Can handle large power
5. Can be used as a switch.
6. Easy to turn on.
7. Can be easily protected with a fuse.

Demerits or disadvantages of SCR

demerits of SCR.

1. Gate has no control, once SCR is turned on.
2. External circuits are required for turning it off.
3. Operating frequencies are low.
4. Additional protection circuits are required.
5. Conducts only in one direction hence controls power during only one half cycle of a.c. input.

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Applications of SCR

the various applications of SCR.

1. Controlled rectifiers.
2. A.C. voltage stabilizers.
3. D.C. to D.C. converters called choppers.
4. D.C. to A.C. converters called inverters.
5. Dimmerstats to control light intensity.
6. For speed control schemes of d.c. and a.c. motors called drives.
7. As a switch.
8. Heater control circuit.
9. In protection circuits.

==========

Explain phase controlled application of SCR. (6 Marks) MQP-1.

- The SCRs conduct in one direction hence can be used in the rectifier circuits. The phase i.e. instant of turning on the SCR can be controlled, to control the average power delivered to the load, using such phase control circuits.
- The Fig. shows circuit for variable resistance phase control using SCR. As shown in the Fig. triggering circuit consists of a diode and resistor in series with the gate. By changing resistor R it is possible to change gate current at specific point on the sine wave. Recall that the SCR is a current operated device and it is the gate current (injected carriers) that turns on the SCR.
- Therefore by changing resistor R, the point on the sine wave at which the SCR fires can be changed, as shown in the Fig. This makes it possible to change the average power delivered to the load.

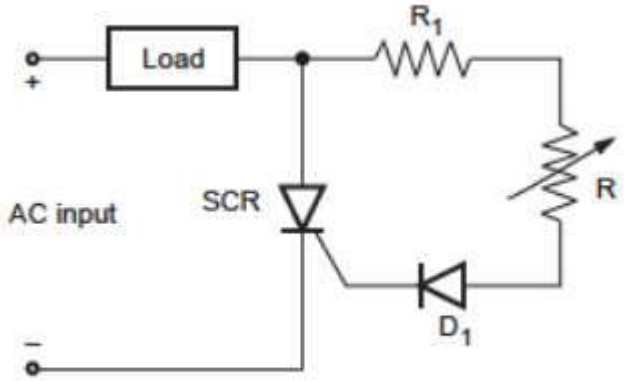

Fig. Variable half wave rectifier

- In the negative half of cycle, SCR is in the reverse blocking state. The diode D_1 in the gate circuit blocks the reverse voltage on the gate.
- As shown in the Fig. 2. , α is a **firing angle** and ϕ is a **conduction angle**. With this gate circuit maximum firing angle we can get is 90°.

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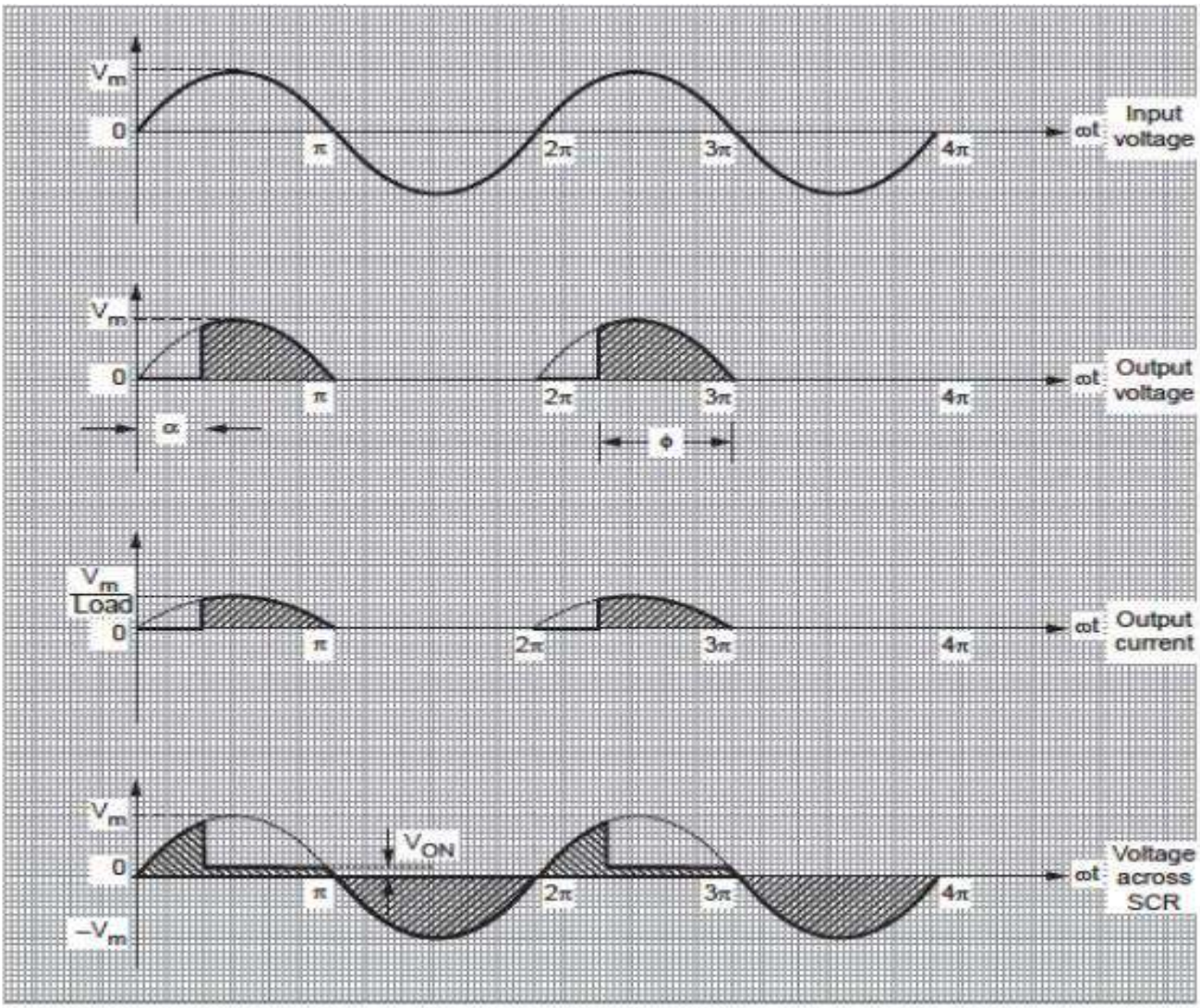

Fig. 2. Waveforms of variable phase control circuit for firing angle α

Note: 1. Fringing angle (α) + conduction angle (ϕ) = 180^0.

2. Maximum Fringing angle is $\alpha_{max} = 90^0$.

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Question Bank

MODULE-3

Operational Amplifiers and Applications

Introduction to Op-Amp, Op-Amp Input Modes, Op-Amp Parameters-CMRR, Input Offset Voltage and Current, Input Bias Current, Input and Output Impedance, Slew Rate (12.1, 12.2 of Text 2)

Applications of Op-Amp- Inverting amplifier, Non-inverting amplifier, Summer, Voltage follower, Integrator, Differentiator, Comparator (6.2 of Text 1)

1. Text 1 : D.P Kothari, I.J Nagarath, "Basic Electronics", 2nd edition, Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

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Part A: Basics of Op-amp

1. Explain the block diagram of an operational amplifier. **(06 Marks) Dec 2018-Jan 2019.**
2. Define the following terms with respect to op-amp.
   i. CMRR
   ii. Slew rate
   iii. µp offset voltage and current
   iv. µp bias current
   v. Supply voltage Rejection Ration
   vi. Common Mode Gain Ac of Opamp
   vii. Input bias
   viii. Input impedance
   ix. Output impedance
   x. Virtual ground

   (08 Marks) Dec 2018-Jan 2019 /(08 Marks) June-July 2019/(08 Marks) Dec 2019-Jan 2020./ MQP-1/ MQP-2/MQP-3
3. A certain op-amp has an open loop voltage gain of 1,00,000 and common mode gain of 0.2. Determine the CMRR and express it in decibles. **(4 Marks) MQP-2**

4. Explain the different µp modes of an op-amp. **(06 Marks) Dec 2018-Jan 2019 .**

5. What is Op-amp? List the characteristics of ideal Op-amp. **(06 Marks) June-July 2019/(06 Marks) Dec 2019-Jan 2020./(6Marks) MQP- 1**

6. Describe the characteristics of basic op-amp. List out its ideal characteristics. **(08 Marks) MQP-2**
7. Explain the different input modes of an OP-AMP. **/(06 Marks) Dec 2019-Jan 2020.**

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Part B: Applications of Op-amp

1. Explain the operation of an op-amp as a non inverting amplifier with neat diagram and waveforms. **(06 Marks) Dec 2018-Jan 2019./ MQP-2**

2. Explain the operation of an Op-AMP as inverting amplifier with neat diagram and waveforms. **/(06 Marks) Dec 2019-Jan 2020./ MQP-1/MQP-3**

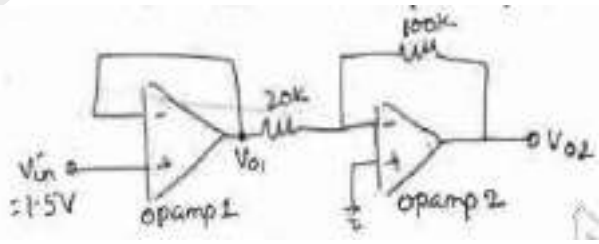
3. Draw the three input inverting summer circuit and derive an expression for its output voltage. **(8 Marks) MQP-1**

4. Derive an expression for the output voltage of an inverting summer. **(06 Marks) MQP-3**

5. A non inverting amplifier circuit has an input resistance of 10KΩ and feedback resistance 60 KΩ with load resistance of 47KΩ. Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is 1.5 Volts. **(08 Marks) MQP-3**

6. Explain op-amp as a subtractor with neat circuit diagram. **(08 Marks) Dec 2018-Jan 2019.**

7. For an op-amp circuit shown in fig. Find the output Vo1 and Vo2. Also write the function of each op-amp used. **(06 Marks) Dec 2018-Jan 2019 /MQP-1**

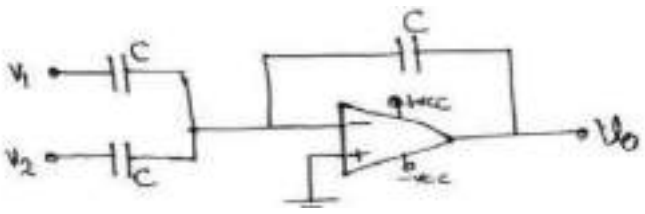


8. Explain how Op-amp can be used as i) Integrator and ii) Voltage follower. **(08 Marks) June-July 2019. /(08 Marks) Dec 2019-Jan 2020./ MQP-2/MQP-3**

9. Explain how op-amp can be used as differentiator. **(06 Marks) June-July 2019./MQP-1**

10. The input to the basic differentiator circuit is a sinusoidal voltage of peak value of 10mV and frequency 1.5 KHz. Find the output if, R_f=100KΩ and C_1=1μF. **(6 Marks) MQP-3**

11. Find the output of the Op-amp circuit shown in Fig. below. **(08 Marks) June-July 2019**



12. Design an Op-Amp circuit to obtain output expression as V_0=- [V_1+3V_2+5V_3]. **(06 Marks) June-July 2019.**

13. Design an adder circuit using Op-Amp to obtain output Voltage as V_0=- [2V_1+3V_2+5V_3] assume R_f=10KΩ (06 Marks) **Dec 2019-Jan 2020./ MQP-1/MQP-2.**

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"Tell me and I Forget, Show me and I remember, Let me do and I Understand"

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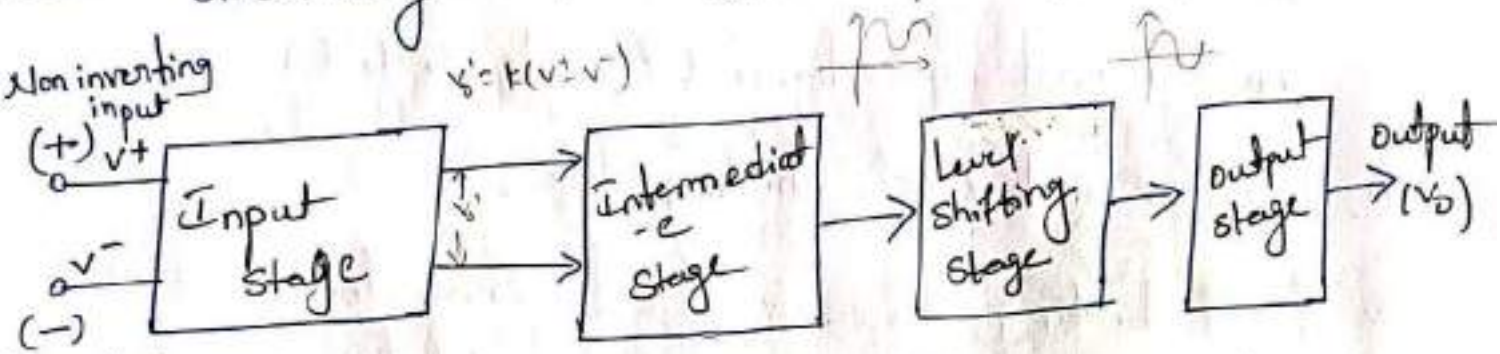
MODULE-3
Part A: Basics of Op-amp

Explain the block diagram of an operational amplifier. (06 Marks) Dec 2018-Jan 2019.

Soln:- Block diagram of a Typical op-Amp



inverting input

- Dual input balanced output differential amplifier R_i

Dual input unbalanced output Differential amplifier (multistage amplifier)

Emitter follower BJT

ideal	Practically
$R_i = \infty$	↑
$R_o = 0$	↓

Push-pull amplifier

A_v ↓ R_o (low) ↓

i. Input Stage :-

* It Consists of a dual input, balanced output differential amplifier.
* it's function is to amplify the difference of two input signals.
* it provides high differential gain, high input impedance (R_i) and Low output impedance.

ii. Intermediate stage :-

* The overall gain requirement of an opamp is very high. Since the input stage alone cannot provide such a high gain.

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* Intermediate stage is used to provide the required additional voltage gain.
* it Consists of another differential amplifier with dual input, and unbalanced (Single Ended) output.

iii. Buffer and Level shifting stage:-

* Level shifting stage is used to bring down the d.c voltage level to Zero with respect to ground potential.
* Buffer is usually an Emitter follower used for impedance matching.

iv. Output Stage:-

it Consists of a push-pull amplifier, which provides o/p (output)

* Large A.C voltage Swing
* Raises current supply capability of OpAmp.
* maintains Low output impedance.

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Define the following terms with respect to op-amp.

- i. CMRR
- ii. Slew rate
- iii. (i/p) µp offset voltage and current
- iv. (i/p) µp bias current
- v. Supply voltage Rejection Ration (or) [PSRR]
- vi. Common Mode Gain Ac of Opamp
- vii. ~~Input bias~~ o/p offset voltage .
- viii. Input impedance
- ix. Output impedance
- x. Virtual ground

(08 Marks) Dec 2018-Jan 2019 /(08 Marks) June-July 2019/(08 Marks) Dec 2019-Jan 2020./ MQP-1/ MQP-2/MQP-3

i. CMRR [Common Mode Rejection Ratio]

CMRR is defined as the ratio of the differential gain 'Ad' to the common mode gain 'Ac'.

$$CMRR = \rho = \frac{A_d}{A_c}$$

CMRR is always expressed in decibles as

$$(CMRR)_{dB} = 20\log_{10}\left(\frac{A_d}{A_c}\right)$$

The typical value of CMRR for MA741 op-amp is 90dB.

* Higher the value of CMRR, better is the ability of the op-amp to reject the common mode signal.

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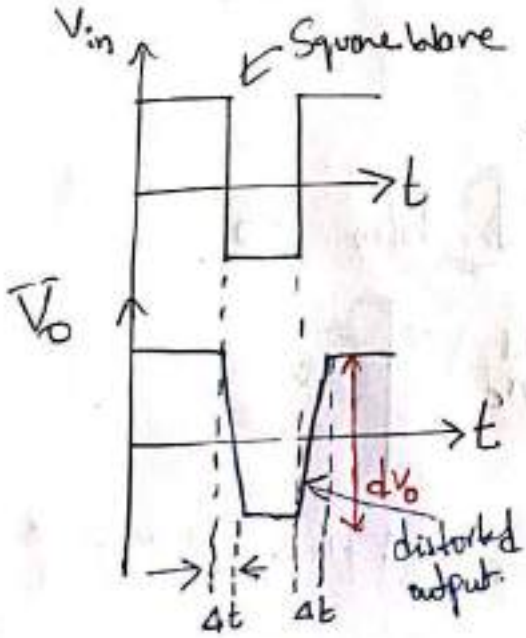
ii. Slew Rate:-

Slew rate of the op-amp is defined as the Maximum rate of change of its output voltage w.r.t time and is expressed in volts per microsecond. (V/μsec)

$$\therefore \boxed{S = \text{slew rate} = \left.\frac{dV_o}{dt}\right|_{max}}$$

* For IC 741 opamp. the slew rate is 0.5 V/μ-sec.

* The ideal value of slew rate is infinite.



Slew Rate Equation:-

* Consider Unity gain opamp circuit with Sinusoidal input

$\therefore \bar{V}_{in} = V_m \sin\omega t$

for unity gain, $\bar{V}_o = \bar{V}_{in} = V_m \sin\omega t$

$$\therefore S = \left.\frac{dV_o}{dt}\right|_{max} = \frac{d(V_m \sin\omega t)}{dt}$$

$$S = \left|\frac{dV_o}{dt}\right| = |V_m \cdot \omega \cdot \cos\omega t|$$ / Maximum value of $|\cos\omega t| = 1$

$$\therefore S = V_m \cdot \omega = V_m(2\pi f)$$

$$\boxed{S = V_m\omega = 2\pi f V_m}$$

* ideally higher the value of S, better is the performance of op-amp.

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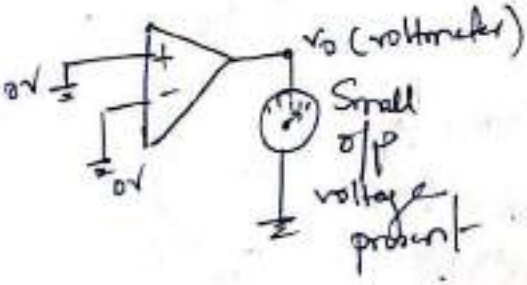
* For free distortion output, the maximum allowable input frequency can be obtained from Slew rate eq^n as,

$$f_m = \frac{S}{2\pi V_m} \quad Hz$$

V_m - peak output voltage.

This is called "full power bandwidth" of the op-Amp.

iii a. Input offset voltage :- (V_{IOS})



* whenever both the input terminals of the opamp are grounded, the practical op-amp shows a small non-zero output voltage. This is due to mismatching present in the internal circuit of the op-amp.

* Such a voltage can cause Error in the practical application for which op-amp is used.

* To make such a voltage zero, it is necessary to apply small difference voltage between the two input terminals of the op-amp. This voltage is called "input offset voltage".

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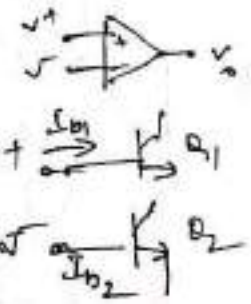
Def^n:-

The differential voltage that must be applied between the two input terminals of an op-amp, to make the output voltage Zero is called "input offset voltage" and denoted as V_{ios}.

* Smaller the value of V_{ios}, better is the matching of the input terminals.
* V_{ios} depends on the temperature.
* for opamp 741, the V_{ios} is 6mVolts.

iii b. Input offset Current:- (I_{ios})



* The algebraic difference between the currents flowing into the two input terminals of the op-amp is called "input offset current" and denoted as I_{ios}.

* $I_{ios} = |I_{b_1} - I_{b_2}|$

I_{b_1} – Current entering into non-inverting terminal.

I_{b_2} – Current entering into inverting terminal.

* Ideally I_{ios} is Zero while for opamp 741, maximum value of I_{ios} is 200nA.

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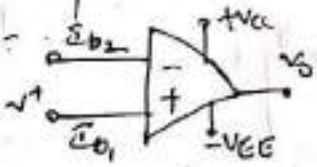
iv. Input Bias Current (I_{bi})

* The average value of the two currents flowing into the op-amp input terminals is called input bias Current and denoted as I_{bi}.



* mathematically $\boxed{I_{bi} = \frac{I_{b_1} + I_{b_2}}{2}}$.
* ideally it should be Zero while for op-amp 741. maximum value of I_b is 500nA.

v. Supply Voltage Rejection Ratio (or) Power Supply Rejection Ratio (PSRR)

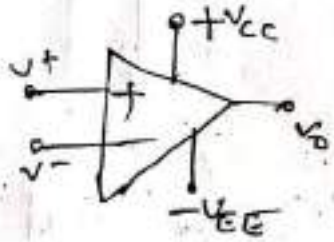
PSRR is defined as the ratio of change in input offset voltage due to change in the supply voltage producing it, keeping other power supply voltage Constant.

* if V_{EE} is Constant $\Rightarrow$ $\boxed{PSRR = \frac{\Delta V_{ios}}{\Delta V_{cc}}\Big|_{V_{EE}\text{-constant}}}$

[Measured in mV/V (or) μV/V.]

(or)

* $\boxed{PSRR = \frac{\Delta V_{ios}}{\Delta V_{EE}}\Big|_{V_{cc}\text{-constant}}}$



* Typical value of PSRR for ãc 741 is 30μV/V.

V_{CC}, V_{EE} } Supply voltages.

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vi. Common Mode Gain (A_c)

* if input voltages of an opamp V_1 and V_2 are equal then ideally output voltage must be zero.
* But the output voltage of a practical differential amplifier not only depends on the difference voltage but also depends on the average common Level of the two inputs.
* ie $\bar{V}_c = \frac{V_1 + V_2}{2}$, where V_c – Common mode signal.
* The gain with which op-amp amplifies the common mode signal to produce the output is called common mode gain of an op-amp denoted as A_c.

$$\bar{V}_o = V_c A_c \qquad A_c = \frac{V_o}{V_c}$$

(A_c ← Common Mode gain.)

Thus there Exists Some finite output for $V_1 = V_2$ due to such Common mode gain A_c, in case of practical op-amps.

* Total output voltage of any Differentially amplifier is total o/p.

$$\bar{V}_o = A_d \bar{V}_d + A_c \bar{V}_c$$

volt'n.

($\bar{V}_d = (V_1 - V_2)$ & $A_d = \frac{V_o}{V_d}$; $\bar{V}_c = \frac{V_1 + V_2}{2}$ & $A_c = \frac{V_o}{V_c}$)

for ideal op-amp $A_d = \infty$, while $A_c = 0$. this Ensures Zero output for $V_1 = V_2$.

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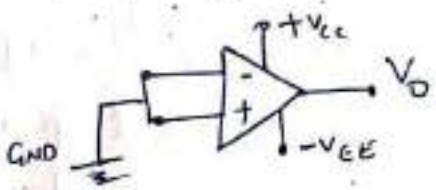
vii. output offset voltage (V_{OOS})



when both the input terminals are shorted and connected to ground, the output should be ideally zero but practically there exists a small dc output voltage known as output offset voltage. (V_{OOS}).

viii. Input impedance (R_i)

* it is the equivalent resistance measured at either the inverting (or) non-inverting input terminal with respect to ground".
* it is denoted as R_i. and must be as high as possible.
* The ideal value of R_i is infinit (∞) but practically for IC 741 in the range of MΩ.

ix. Output impedance (R_o)

* it is the equivalent resistance Measured between the output terminal of the op-amp with respect to ground.
* its value must be as Low as possible. (ideally Zero).
* it is denoted as R_o and for op-amp 741 it is 75Ω.

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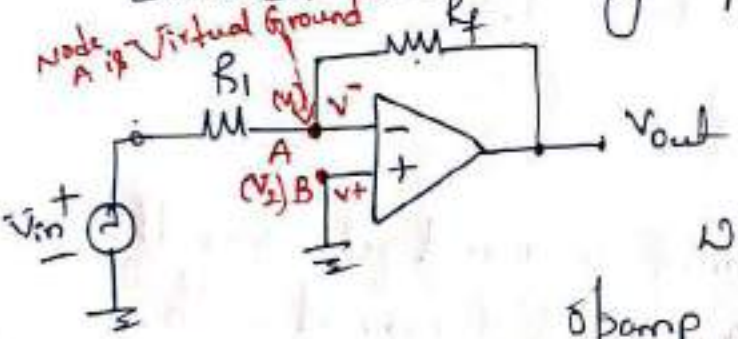
x. Virtual ground :-

Whenever the op-amp operated in Negative feed back (closed Loop mode) mode the potential at inverting and Non inverting terminals are equal.

ie. $\boxed{V^+ = V^-}$

Consider the inverting amplifier



potential at node A (V_1) = potential at node B (V_2).

W.k.t the differential gain of a opamp $A_d = \frac{V_o}{V_d}$

$$V_d = \frac{V_o}{A_d}$$

Differential input voltage $(V_1 - V_2)$ ← ideally it is ∞ for opamp.

$$V_d = \frac{V_o}{\infty} = 0$$

ie $(V_1 - V_2) = 0$

$$\Rightarrow \boxed{V_1 = V_2}$$ proved. ie $V^+ = V^-$

Virtual Ground Concept is Very useful in analysis of an op-amp when negative feedback is employed. it will Simplify a Lot of Calculations and derivations.

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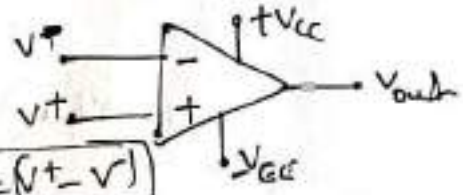
Gain

opamp - open Loop Gain :-

(a) Differential gain :-

* it is the ratio of output voltage to the differential input voltage, when op-amp is in open-Loop configuration, without any feedback.
* it is also called large signal voltage gain (or) open Loop gain and denoted as A_{OL}.



$V_d = (V+ - V-)$

$$A_{OL} = \frac{V_o}{V_d}$$

$$A_d = \frac{V_o}{V_d}$$

$$(A_d)_{dB} = 20\log\left(\frac{V_o}{V_d}\right)$$

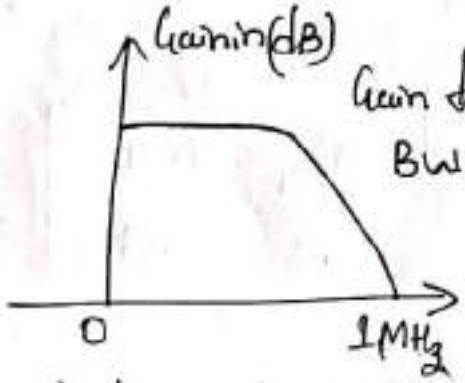
* For op-amp 741 IC, it is typically 2,00,000.

Gain - Bandwidth product (unity) (GBWP)

* it is the BW (frequency) of op-amp when voltage gain is unity (ie 1).
* The gain is generally expressed in dB. Thus unity gain has dB value $20\log(1) = 0$ dB.

$GBWP = 10^6$

i.e $\boxed{\text{Gain} \times BW = 10^6}$



* it is about 1MHz for opamp 741.
* The gain bandwidth product is also called Unity gain Bandwidth (UGB) or closed Loop B.W.

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A certain op-amp has an open loop voltage gain of 1,00,000 and common mode gain of 0.2. Determine the CMRR and express it in decibles. **(4 Marks) MQP-2**

Soln:-

$A_{OL} = 1,00,000 = A_d$.

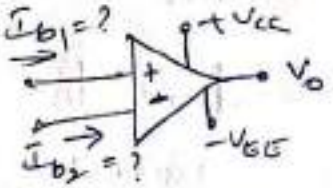
$A_C = 0.2$.

$$CMRR = \frac{A_d}{A_C} = \frac{1\times10^5}{0.2} = 5\times10^5$$

$$(CMRR)_{dB} = 20\log(A_d/A_C) = 20\log(5\times10^5)$$

$$\boxed{(CMRR)_{dB} = 113.979 \simeq 114\ dB}$$

Problem. For a particular op-amp, the input offset current is 20nA while input bias current is 60nA. Calculate the values of two input bias currents.



Soln:-

$$I_{ios} = 20nA = I_{b_1} - I_{b_2} \leftarrow (1)$$

$$I_b = 60nA = \frac{I_{b_1} + I_{b_2}}{2} \leftarrow (2)$$

$$I_{b_1} - I_{b_2} = 20\times10^{-9}$$

$$I_{b_1} + I_{b_2} = 120\times10^{-9}$$

Solving

$$2I_{b_1} = 140\times10^{-9}$$

$$\boxed{I_{b_1} = 70\times10^{-9}}$$

$$\boxed{I_{b_1} = 70nA}$$

$$\boxed{I_{b_2} = 50nA}$$

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Explain the different µp modes of an op-amp. **(06 Marks) Dec 2018-Jan 2019.**

Explain the different input modes of an OP-AMP. **/(06 Marks) Dec 2019-Jan 2020.**

Soln:- input modes of an Op-amp are

i. Single-Ended differential Mode.

ii. Double ended differential mode.

iii. Common mode.

i. Single-Ended differential mode:-

* When an opamp is operated in the Single ended differential mode, one input is grounded and a voltage Signal is applied to ther other input.

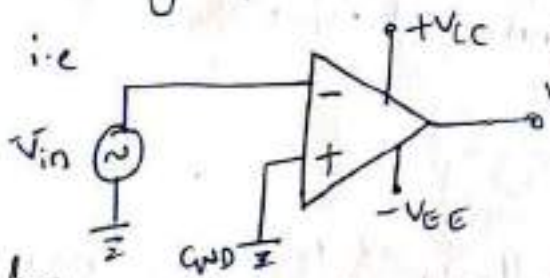

fig a Single Ended inverting mode

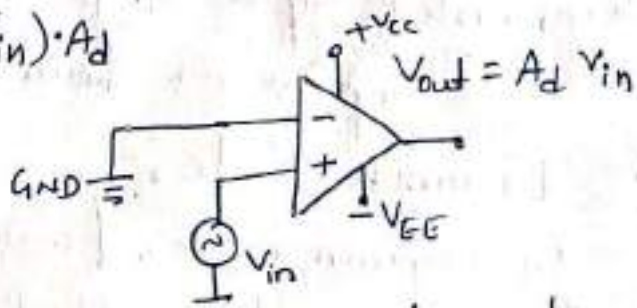

fig b. Single Ended Non-inverting Mode

fig:- Single Ended differential Mode.

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ii. Double Ended (or) differential Mode:-

* Two opposite-polarity (out-of phase) Signals are applied to the inputs.
* The output of opamp V_{out} is amplified version of difference between two input Signals.

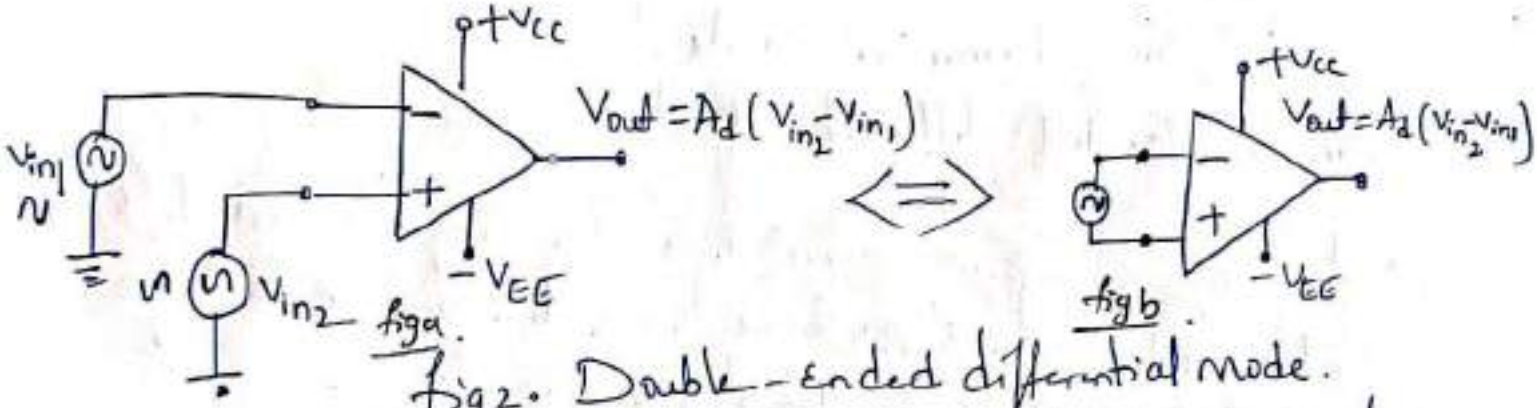


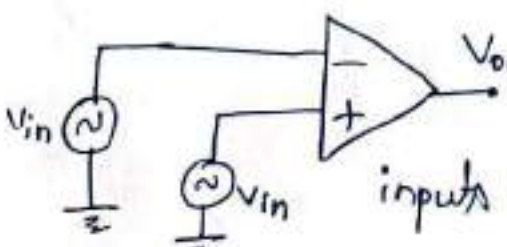
fig a. fig b.

fig 2. Double-ended differential mode.

* Equivalently, double-ended differential Mode can be represented by a single source connected b/w the two inputs as shown in fig b:

iii. Common Mode:-

* In Common mode, two Signal voltages of the same phase, frequency, and amplitude are applied to the two inputs.
* When Equal input signals are applied to both inputs, they tend to cancel, resulting a Zero output voltage.
* This action is called Common mode rejection



$V_{out} = 0$, its importance lies in the situation where an unwanted signals appears commonly on both inputs (noise). This unWanted Signal will not appear on the o/p and distor the desired signal.

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What is Op-amp? List the characteristics of ideal Op-amp. (06 Marks) June-July 2019/(06 Marks) Dec 2019-Jan 2020./(6Marks) MQP- 1

Describe the characteristics of basic op-amp. List out its ideal characteristics. (08 Marks) MQP-2

Soln:- opamp is direct coupled multistage voltage amplifier with very high gain. it has very high input impedance and a very Low output impedance.

i. Infinite Voltage gain ($A_{OL} = \infty$)

The open loop voltage gain of opam (A_{OL}) of ideal opamp is infinity.

i.e $A_{OL} = \infty$.

ii. Infinite input impedance ($R_i = \infty$).

An ideal opamp doesnt draw any current from the voltage Source connected to its input terminals. Thus its input impedance is infinite. ie $\boxed{R_i = \infty}$

iii. Zero output impedance ($R_{out} = 0$).

The output voltage of an ideal opamp is independent of the current drawn from it. this means opamp has Zero output impedance.

i.e $\boxed{R_o = 0}$.

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iv. Infinite Bandwidth ($BW = \infty$).

An ideal opamp amplifies signals of any frequency with a constant gain, which implies that op-amp has infinite B.W. i.e $\boxed{BW = \infty}$.

v. infinite CMRR ($\rho = \infty$) :-

$$CMRR = \rho = A_d/A_c = \frac{\text{differential Gain}}{\text{Common mode gain}}.$$

The common mode rejection ratio of an ideal opamp is infinite. i.e $CMRR = \infty$.

vi. Infinite Slew rate ($SR = \infty$)

ideal opamp has Infinite slew rate this implies that the o/p voltage changes simultaneously with the input voltages.

vii. The characteristics of an ideal op-amp dont change with temperature.

viii. The power supply rejection ratio of an ideal opamp is Zero i.e ($PSRR = 0$)

ix. Zero off-set voltage :-

The presence of small output voltage when $V_1 = V_2 = 0$. is called an offset voltage.

for an ideal op-amp, offset voltage is Zero.

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Table :- Summary :- parameters of ideal and practical (IC 741) opamp.

parameter	Ideal opamp	practical Opamp (IC741)
1. Voltage Gain (A_{OL})	∞	$\simeq 2\times10^5$ ↑
2. input impedance (R_{in}) in Ω	∞	$\simeq 10^6$ ↑
3. Output impedance (R_o) in Ω	0	75Ω. ↓
4. Bandwidth (BW) in Hz	∞	10^6 ↑
5. CMRR	∞	90dB. ↑
6. Slew rate (V/sec)	∞	$\simeq 10^6$ V/sec ↑ (or) → 0.5V/μsec
7. i/p off set Voltage	Zero	6mV (Low) ↓ must be
8. PSRR	Zero	30μV/V. (↓ must be low)
9. i/p bias Current (I_b) = $\frac{I_{b1}+I_{b2}}{2}$	Zero	500nA ↓
10. i/p offset Current $I_{os} = \lvert I_{b1}-I_{b2}\rvert$	Zero	200nA. ↓

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Problem An opamp has a slew rate of 0.5 V/μsec.

i. What is the Maximum undistorted Sine wave which can be produced at a $f = 6.631$ kHz ?

ii. what is the Maximum frequency of the Sine wave that op-amp can be produce at the output without distortion with peak Value of 7 volts ?

bcz $1\mu = 10^{-6}$

Soln: i.. $S = 0.5\,V/\mu sec. = 0.5 \times 10^{+6}$ V/sec

$f = 6.631$ kHz , $V_m = ?$

$S = 2\pi f \cdot V_m \Rightarrow V_m = \frac{S}{2\pi f} = \frac{0.5 \times 10^6}{2\pi \times 6.631 \times 10^3}$

$$\boxed{V_m = 12 \text{ volts}}$$

ii. $f_m = ?$ $V_m = 7$ volts , $S = 0.5 \times 10^6$ V/sec

$$f_m = \frac{S}{2\pi \cdot V_m} = \frac{0.5 \times 10^6}{2\pi \times 7}$$

$$\boxed{f_m = 11.3682 \text{ kHz}}$$

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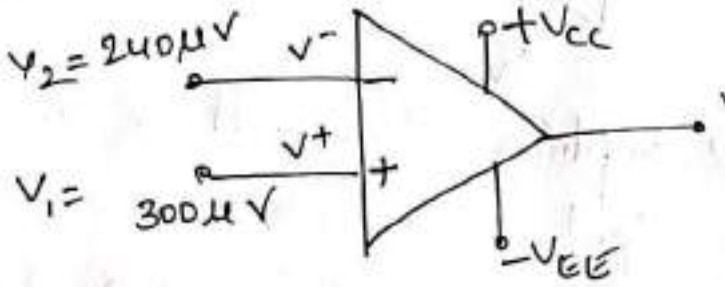
problem.

Determine the output voltage of an opamp for the input voltages of 300μV and 240μV. The differential gain of the amplifier is 5000 and the value of the CMRR is 10^5.

Soln:-



$$V_{out} = A_d(V^+ - V^-) + A_c V_c$$

$$= A_d(V_1 - V_2) + A_c V_c$$

$A_d = 5000$, and $CMRR = 10^5 = \frac{A_d}{A_c}$

$$V_{out} = A_d V_d + A_c \cdot V_c$$

$$A_c = \frac{A_d}{CMRR} = \frac{5000}{10^5} = \frac{[5]}{100} = 0.05$$

$$V_d = (V_1 - V_2) = 300\mu - 240\mu = 60\mu \text{ volts}$$

$$V_c = \frac{V_1 + V_2}{2} = \frac{300\mu + 240\mu}{2} = 270\mu \text{ volts}$$

$$V_{out} = A_d V_d + A_c V_c$$

$$= (5000)(60\mu) + (0.05)(270\mu)$$

$$= 0.3 + 0.135\,m$$

$$= 300\,m + 0.135\,m$$

$A_d V_d$ $\quad$ $A_c V_c$

$\boxed{V_{out} = 300.0135 \text{ m volts}}$

Ideally A_c must be Zero and o/p should be only $A_d V_d$ which is equal to 300mV. Higher the value CMRR, the o/p closer to its ideal value.

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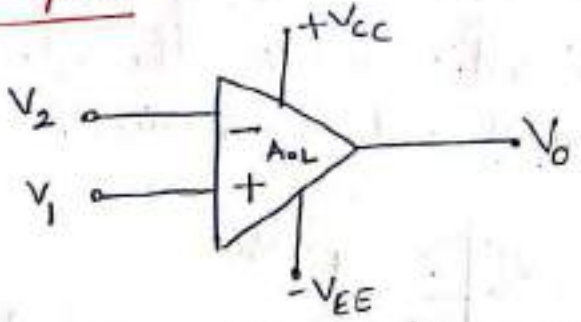
Open-Loop amplifier



In open Loop amplifier, there will be no feedback signal from output to input.

The output voltage is $V_{out} = A_{OL}(V_1 - V_2)$

Closed Loop amplifier :-

Question: Explain why closed Loop Configuration of op-amp is used in all the practical amplifier Circuit and bring out the advantages of closed Loop operation with negative feedback.

Soln:-

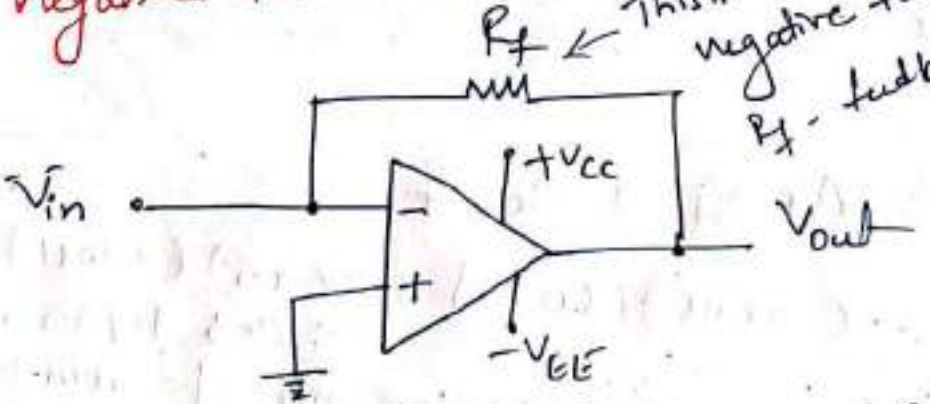


fig:- Op-amp with negative feedback.

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* The closed Loop amplifier is possible using feedback. i.e feeding some part of the output back to the input through resistor. always op-amp is used with negative feedback.
* The gain resulting with feedback is called closed Loop gain of the op-amp. Due to -ve feedback gain decreases.

Advantages of -ve feedback:-

i. it reduces the gain and makes it controllable.
ii. it reduces the distortion.
iii. it increases the Bandwidth.
iv. it increases the input resistance (R_i) of the op-amp. ↑
v. it decreases the output resistance (R_o) of the op-amp. (↓).
vi. it reduces the effect of temperature and power Supply.

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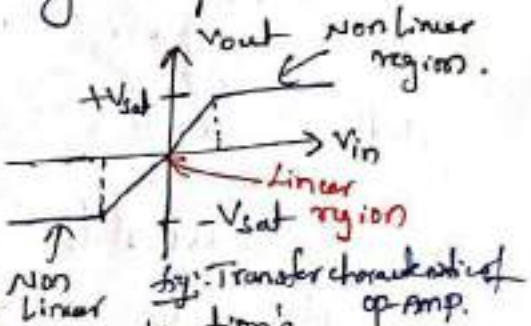
Question. Applications of opAmp:-
what is an opamp? Mention some of the applications. State the reason for its wide spread applications.

Soln:- "op-Amp is a directly Coupled multi-stage voltage amplifier with high gain. it has very high input impedance and a very low output impedance."

* An operational amplifier (or an op-Amp) is an integrated Circuit (IC) that operates as an voltage amplifier.



OpAmp Applications:

Linear Applications: ($V_{out} = KV_{in}$)

Eg:
* Amplifiers (Inv & Non-Inv)
* Adder
* Subtractor
* voltage follower
* Current to voltage Convertor
* voltage to Current Convertor
* Integrator
* Differentiator
* Active filters (LPF, HPF, BPF, BSF)
* Instrumentation Amplifier

Non-Linear applications: ($V_{out} = \{\pm V_{sat}\}$ (Switching Mode))

Eg:
* Comparator
* Logarithmic amplifier
* Exponential amplifier
* peak detector
* Zero Crossing detector
* Precision rectifier
* waveform generators
* clippers & clampers.
* Schmitt trigger (Zero crossing detector with +ve feedback)
* multivibrators.

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Reason for Wide Spread Applications :-

i. Very high gain
ii. Very large Bandwidth (BW).
iii. High input impedance (R_i)↑
iv. Very Low output impedance (R_o)↓.
v. Low cost and Available in I.C.
vi. Characteristic of op-Amp are independent of temperature.

Voltage Levels and Saturation property of Op-Amp

Question: what is Saturating property of an op-Amp ? Mention the typical value of Saturating output voltage for an IC 741 op-Amp operating at ±12V DC supply.

Soln:-
* Saturation property of an op-Amp in which the output voltage Swinging between saturation voltages ie $\pm V_{sat}$.
* Thus if output tries to rise more than $+V_{CC}$ (or) less than $-V_{EE}$ then it gets clipped and gets Saturated at the levels almost equal to $+V_{CC}$ and $-V_{EE}$.

ie $V_{out(max)} \leq \pm V_{sat}$ → $+V_{sat} \leq +V_{CC}$, $-V_{sat} \leq -V_{EE}$

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* Practically the saturation voltage levels are about 90% of the supply voltage levels.

$$V_{out(Practical)} = 0.9\,(V_{supply\ voltage})$$

Thus for an op-amp of supply ±12V, then the Saturation voltage levels are 90% of ±12V i.e ±10.8 volts.

Ex: If V_{supply} is ±15V then the saturation voltage levels are $0.9(\pm 15V) = \pm 13.5$ volts.

* Ideally it is Considered that the output voltage of the op-amp saturates at $+V_{cc}$ and $-V_{EE}$ levels.

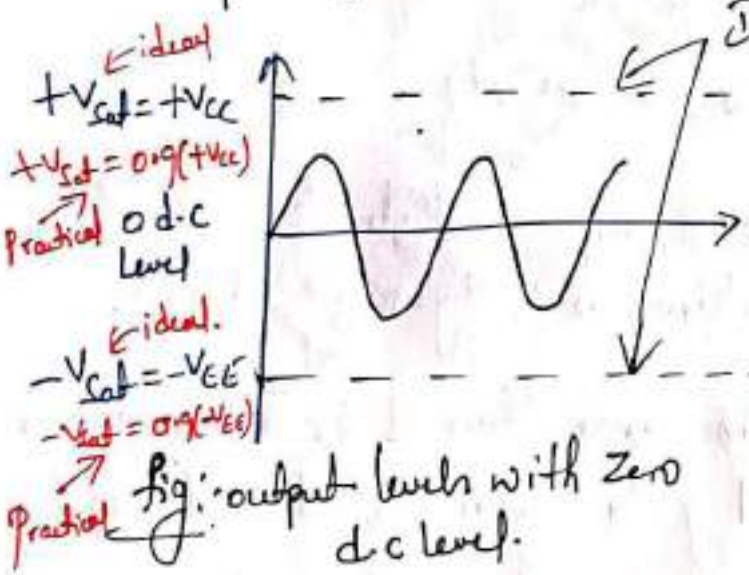

fig: output levels with zero d.c level.

* output of an op-amp Saturates if tries to increase more than its supply voltages.

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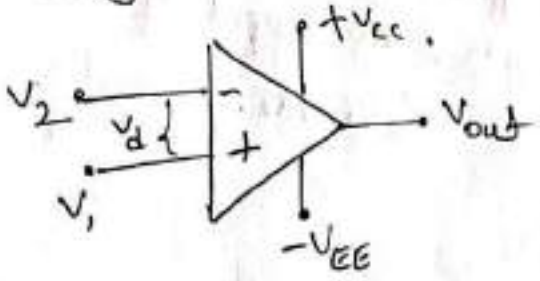
For Example:-

Consider an op-amp having gain $A_{OL} = 10^5$ and supply voltages $\pm 12V$.



$$V_d = V_1 - V_2$$

$$V_{out} = A_{OL} \cdot V_d$$

$$V_d = \frac{V_{out}}{A_{OL}}$$

$V_{out} = \pm V_{sat} = \pm 12V$ in ideal condition.

$$\therefore V_d = \frac{\pm V_{sat}}{A_{OL}} = \frac{\pm 12}{10^5} = \pm 12 \times 10^{-5} = \pm 120 \times 10^{-6} \text{ volts}$$

$$V_d = \pm 120\mu \text{ volts}$$

∴ The differential input to the op-amp must be Lenthan $\pm 120\mu$ volts to avoid clipping of the output waveform.

$> (120\mu \text{ volts})$

Let assume. $V_d = 1mV$ (Sine wave)

$$V_{out} = V_d \cdot A_{OL}$$
$$= 1 \times 10^{-3} \times 10^5$$

$V_{out} = 100$ volts ✗ (Expected) (not possible practically bcz it Exceeds $\pm V_{sat}$)

∴

$$V_{out} = \pm 12 \text{ Volts} = \pm V_{sat}$$

the o/p voltage above +12V & below −12V will be clipped off due to Saturation property of opamp.

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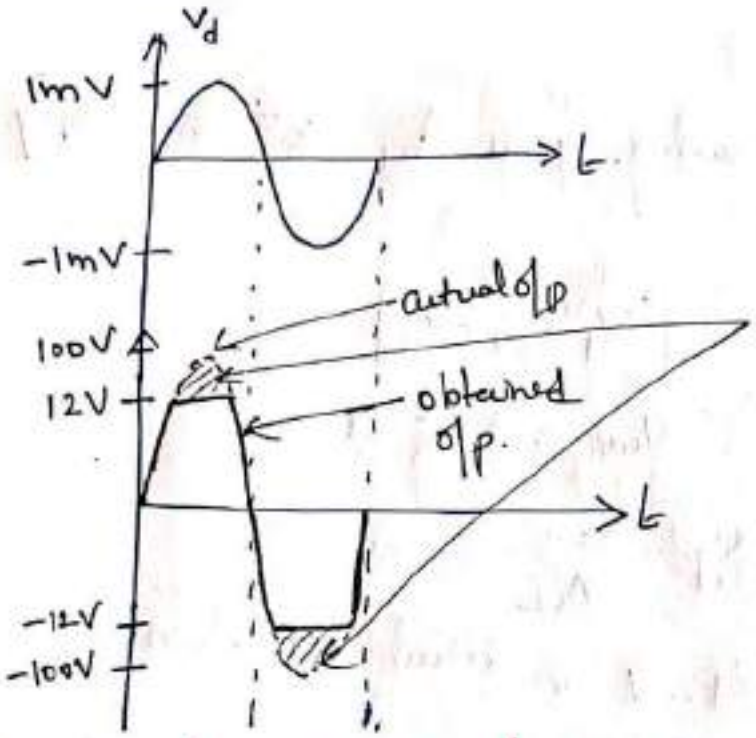

o/p voltage above 12V and below -12V is clipped o/p due to saturable property.

Transfer characteristics of Opamp [V_{out} v/s V_d]

The graph of output voltage V_{out} plotted against the differential input voltage (V_d) assuming gain Constant is called voltage transfer curve (or) characteristics of op-amp.

Ex: Ideal voltage transfer curve.

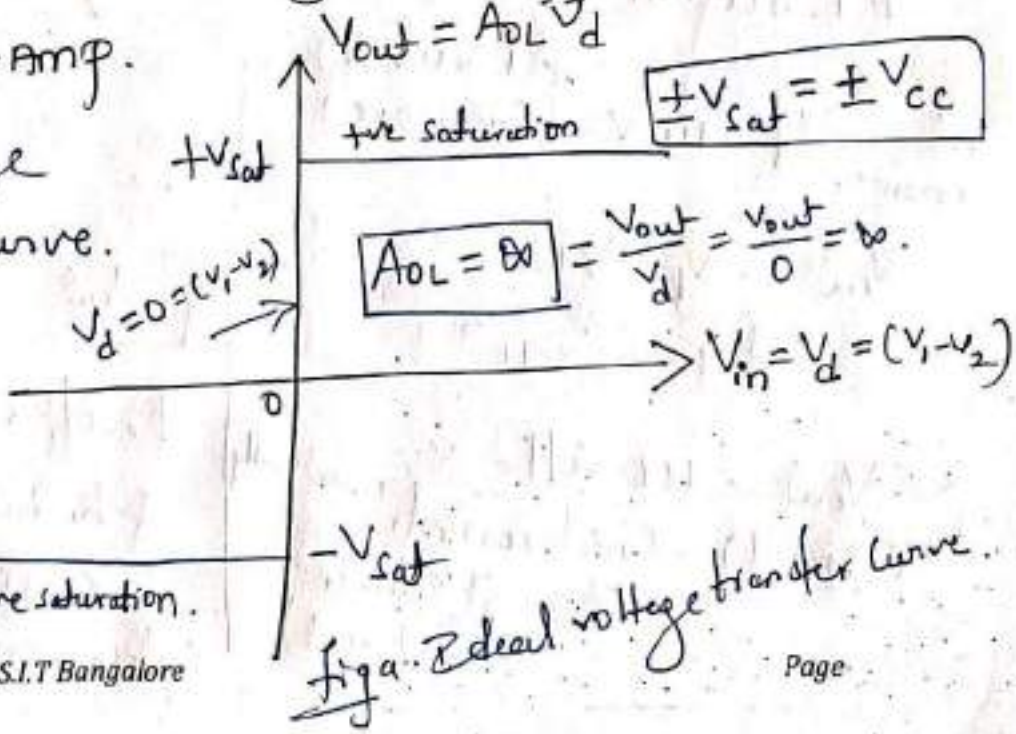

Fig a. Ideal voltage transfer curve.

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Thus for Zero input ($V_d = 0$), the output of op-amp is always at Saturation Level $\pm V_{sat}$ due to infinite gain. Thus voltage transfer Curve for ideal op-amp is a vertical line as shown in fig a.

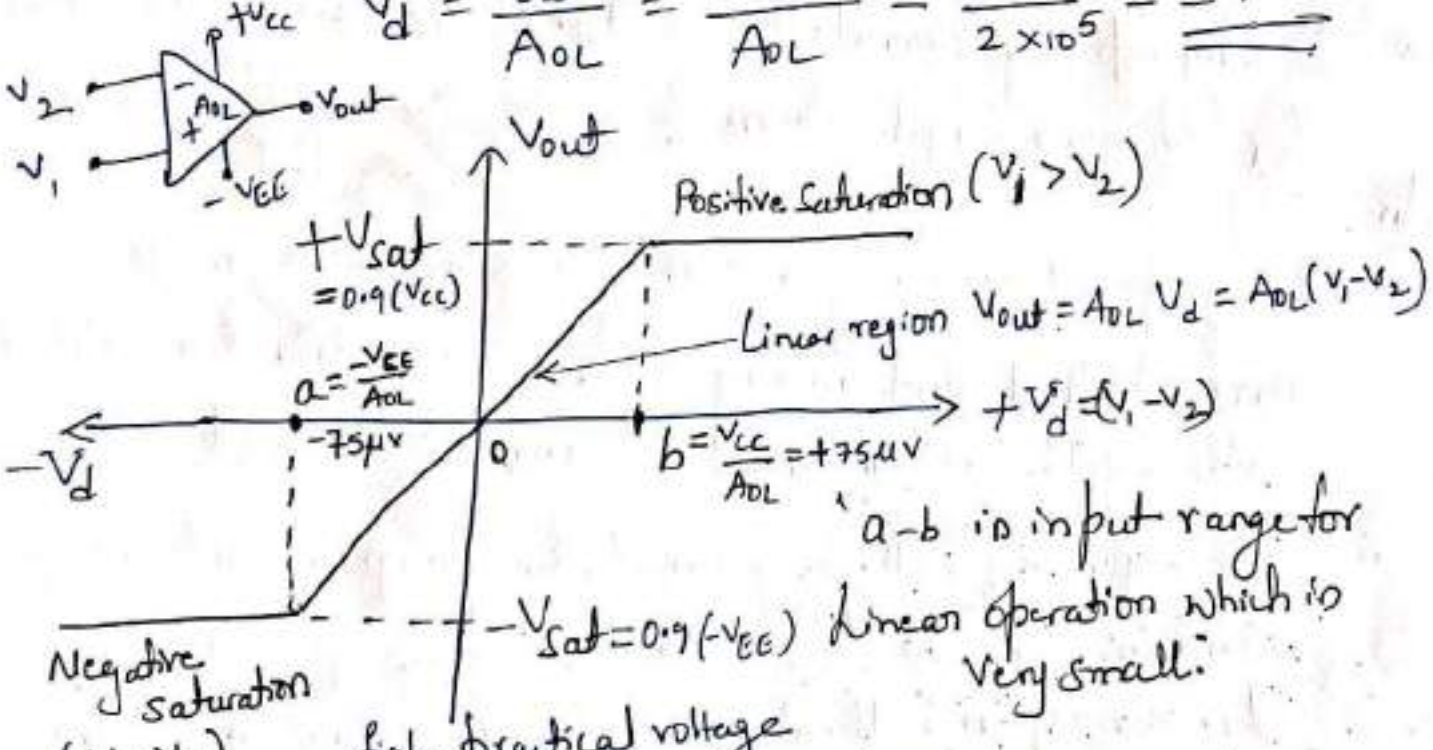
* Thus ideally range of input for Linear operation of the op-Amp is Zero.

ii. Practical voltage Transfer Curve:-

Practically A_{OL} is finite for the opamp. for opamp 741 IC it is 2×10^5.

$V_{out} = A_{OL} \cdot V_d$ & $\Rightarrow$ $V_{out} = \pm V_{sat} = \pm 15\,V$

$$V_d = \frac{V_{out}}{A_{OL}} = \frac{\pm V_{sat}}{A_{OL}} = \frac{\pm 15V}{2 \times 10^5} = \pm 75\mu V$$



a-b is input range for Linear operation which is very small.

fig b. practical voltage transfer curve.

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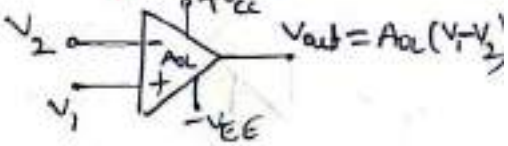
* Hence practically till V_d is between $-75\mu V$ and $+75\mu V$, the output will vary Linearily with input. But once V_d Exceeds $\pm 75\mu V$, the output is saturated.
* Thus the practical voltage transfer Curve is as shown in fig b.

i. if V_d is greater than corresponding to b, the output attains $+V_{sat}$.

ii. if V_d is Less than corresponding to 'a', the output attains $-V_{sat}$.

iii. Thus range a-b is input range for which the output varies Linearily with input. But as A_{OL} is very high practically this range is very small $[V_{out}=A_{OL}V_d]$.

Question: Why op-amp cannot be used in open loop configuration for Linear applications?



Soln: Reasons

i. In open loop configuration, the gain of the opamp is uncontrolled and is very high. To control this, feedback path with a resistance is crucial for amplification.

ii. The open loop voltage gain of an opamp is $\simeq 10^6$, a huge number. So, to see that the opamp operates in its Linear region without going to its Saturation region

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ii. (Continued)

, the input voltage should be less than $\frac{V_{cc}}{10^6}$ which is very small number. for example if $V_{cc} = 12$ Volts then input voltage should be $< \frac{12}{10^6} = 12\mu$ volts.

This small voltage can't handled by us. Most of the normal CRO's can't reliably show on their screen voltages less than 2mV.

For these Reasons, opamp is almost always used in closed loop configuration if it is needed in an Amplifier mode.

Definition of op-amp and Why the name OPERATIONAL Amplifier:

Defn:- 'op-amp is a directly coupled multi-stage voltage amplifier with high gain. it has very high input impedance and very low output impedance'.

Why?

op-amps are used for performing various mathematical operations such as additions, subtraction, multiplication, integration and differentiation etc.. thus it is called operational amplifier.

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Pin diagram:-

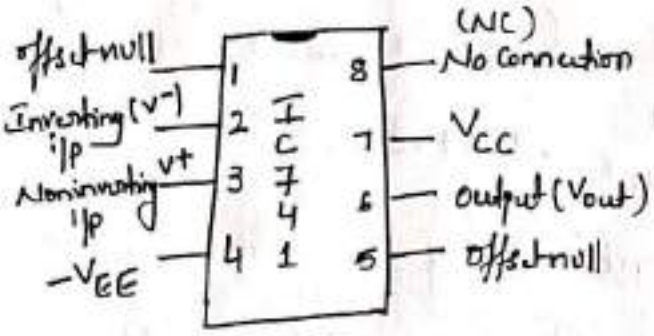
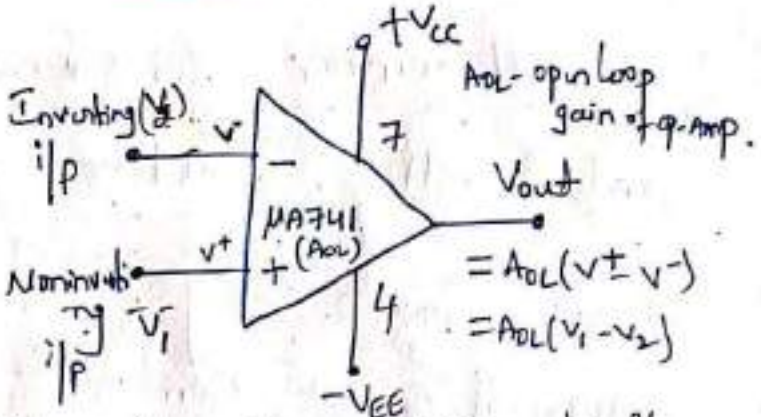


fig:- pin diagram of IC 741.

Symbol:



- ✓ V_1 (or) V^+ is the voltage at noninverting i/p.
- ✓ V_2 (or) V^- is the voltage at inverting i/p.
- ✓ V_{out} - output voltage.

* The output voltage V_{out} is proportional to the difference b/w the input voltage.

i.e $$V_{out} = A_{OL}(V^+ - V^-) = A_{OL}(V_1 - V_2)$$

A_{OL} - open Loop gain of op amp.

Equivalent Circuit of practical op amp:-

* The Circuit which represents op-amp parameters in terms of physical components for the analysis purpose is called Equivalent Circuit of an op-Amp.

* The Equivalent Circuit of an op-amp is shown in fig a.

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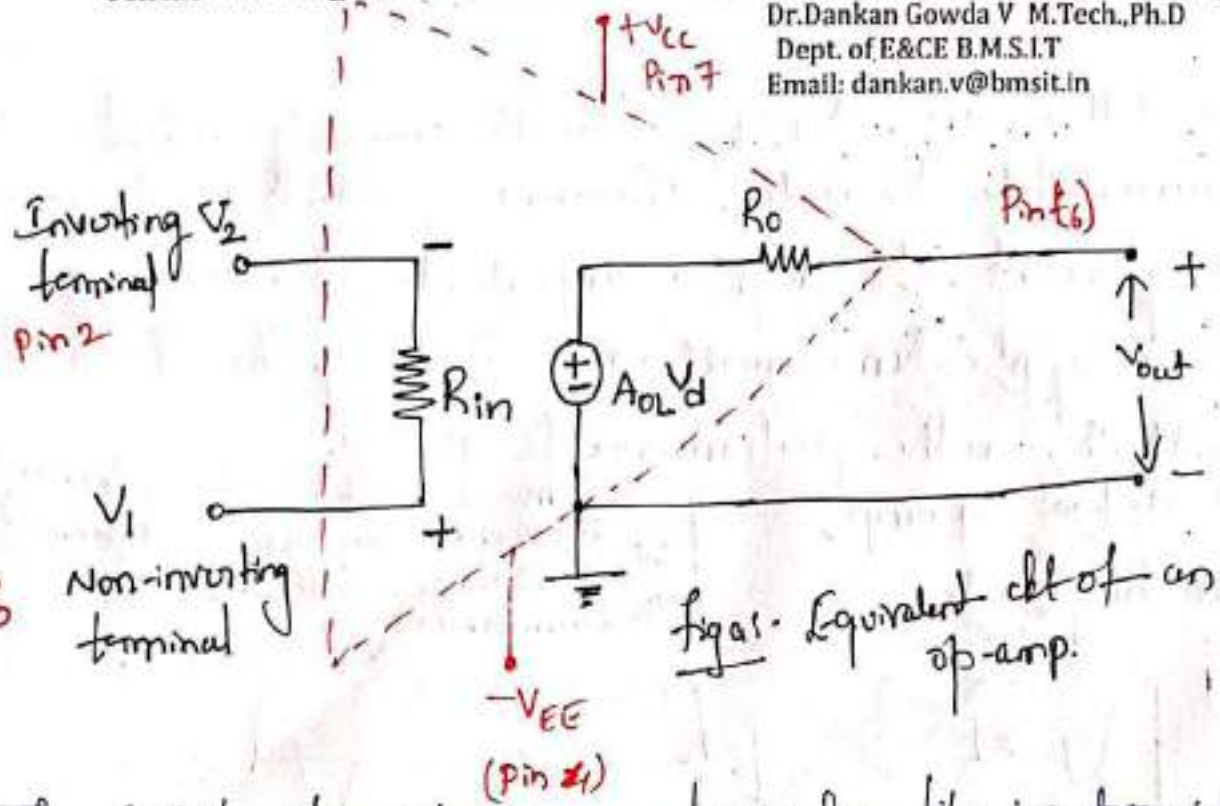

fig 1. Equivalent ckt of an op-amp.

* The circuit shows the op-amp parameters like input resistance (R_{in}), Output resistance (R_{out}), the open Loop voltage gain A_{OL}.
* The op-amp amplifies the difference between two input voltages.

$$V_{out} = A_{OL} \cdot V_d = A_{OL}(V^+ - V^-) = A_{OL}(V_1 - V_2)$$

where A_{OL} – open Loop voltage gain.
V_d – difference voltage $(V_1 - V_2)$
V_1 – voltage at Non-inverting terminal w.r.t ground.
V_2 – voltage at inverting terminal w.r.t ground.
R_i – input resistance of opamp.
R_o – output resistance of opamp.

* The output voltage is directly proportional to the difference voltage V_d.
* it is to be noted that the opamp amplifies difference voltage not the individual input voltages. Thus the output polarity gets decided by the polarity of the difference voltage V_d.

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* The Voltage Source $A_{OL}V_d$ is the Thevenin's equivalent voltage Source while R_o is the Thevenin's equivalent resistance.
* The equivalent ckt plays an important role in analysing various applications as well as in studying the effects of feedback on the performance of op-amp.

Input Modes of op Amp:-

i: Inverting Mode.
ii: Non Inverting Mode } Single ended differential mode.
iii: Double ended Differential mode
iv: Common mode

i. Inverting Mode:-

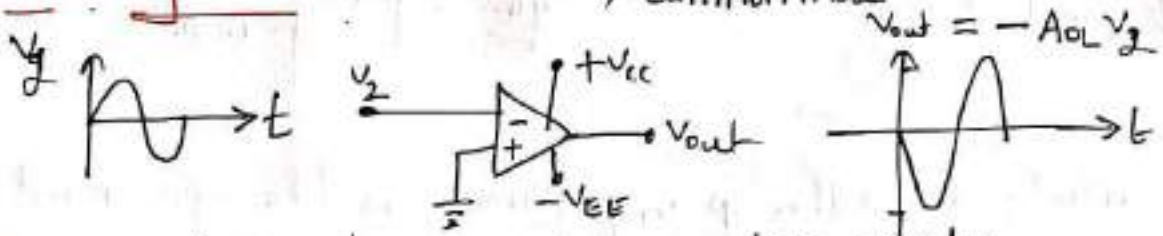


fig a. Op-amp open loop inverting amplifier

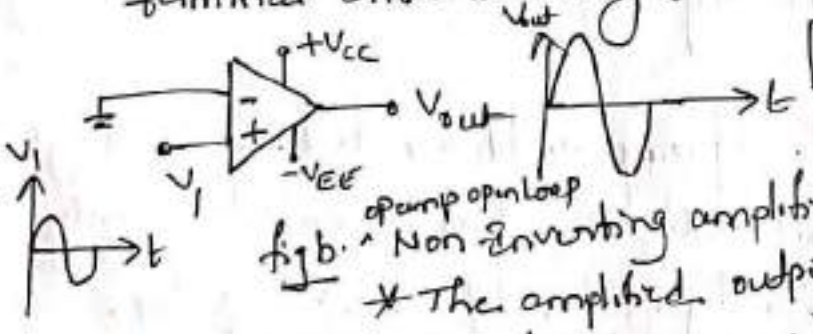
* Inverting mode input is applied to the inverting terminal and non-inverting terminal in grounded.
* The amplified voltage is 180° out of phase w.r.t applied i/p voltage.

i.e $V_{out} = -A_{OL}V_2$

-ve sign indicates that output is 180° out of phase.

ii. Non-inverting mode:-

* In non-inverting mode, i/p is applied to the non-inverting terminal and inverting terminal in grounded.



$V_{out} = V_1 \cdot A_{OL}$

fig b. opamp open loop Non Inverting amplifier

* The amplified output voltage is in-phase w.r.t applied input voltage. i.e $V_{out} = A_{OL}V_1$

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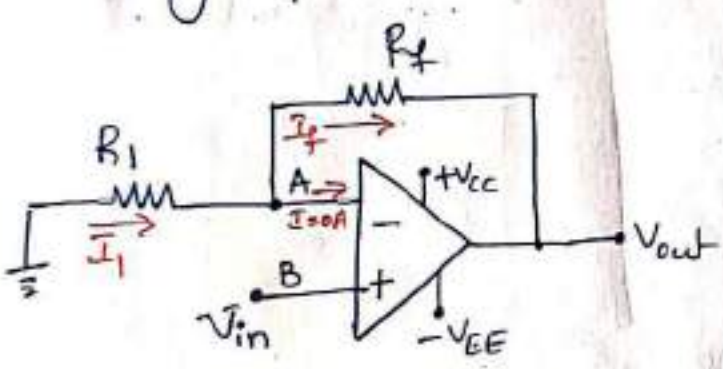
Part B: Applications of Op-amp

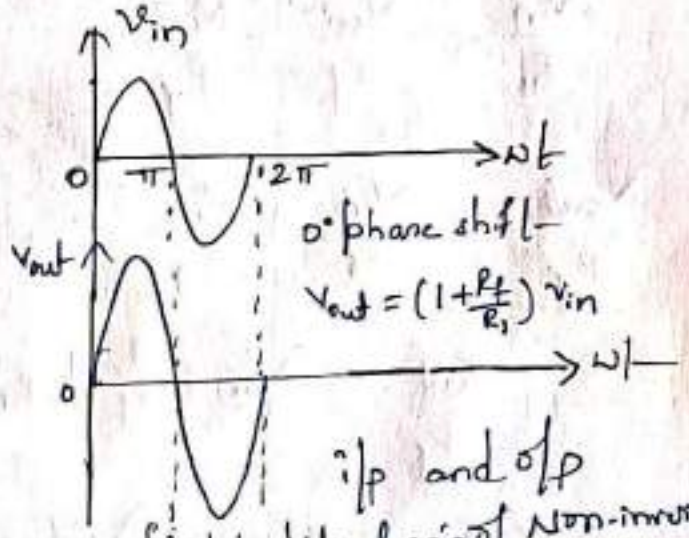
Non-Inverting Amplifier

Q: Explain the operation of an op-amp as a non inverting amplifier with neat diagram and waveforms. **(06 Marks) Dec 2018-Jan 2019./ MQP-2**

* An Amplifier which amplifies the input without producing any phase shift between input and output is called Non-inverting amplifier.
* The Basic Circuit diagram of a non-inverting amplifier using op-amp is shown in the figa.



figa. Non-Inverting Amplifier
R_1 - input Resistance.
R_f - feedback Resistance



figb:- Waveforms of Non-inverting amplifier.

* The input is applied to the non-inverting input terminal of the op-amp.
* The node B is at potential V_{in}, hence the potential of point A is same as B which is V_{in}, from the Concept of Virtual ground.

i.e $\boxed{V_A = V_B = V_{in}}$

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KCL at Node A

$$I_1 = I_f$$

$$\frac{0 - V_A}{R_1} = \frac{V_A - V_{out}}{R_f}$$

W.K.T $V_A = V_{in}$

$$\frac{0 - V_{in}}{R_1} = \frac{V_{in} - V_{out}}{R_f}$$

$$-\frac{V_{in}}{R_1} = \frac{V_{in}}{R_f} - \frac{V_{out}}{R_f}$$

$$\frac{V_{out}}{R_f} = \frac{V_{in}}{R_f} + \frac{V_{in}}{R_1}$$

$$\frac{V_{out}}{R_f} = V_{in}\left(\frac{1}{R_f} + \frac{1}{R_1}\right)$$

$$\frac{V_{out}}{R_f} = \left(\frac{R_1 + R_f}{R_f R_1}\right) \cdot V_{in}$$

$$\frac{V_{out}}{V_{in}} = \left(\frac{R_1 + R_f}{R_1}\right) \Rightarrow \boxed{\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_1} = A_{v_f}}$$

$$\boxed{V_{out} = \left(1 + \frac{R_f}{R_1}\right) V_{in}}$$

Voltage gain of Non inverting Amplifier $\boxed{A_{v_f} = \left(1 + \frac{R_f}{R_1}\right) = \frac{V_{out}}{V_{in}}}$

Note:- Non-Inv. amplifier.

i. gain $A_v = 1 + \frac{R_f}{R_1}$

ii. 0° phase shift b/w input and output.

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Question.

Draw the non-inverting voltage amplifier circuit using an op-amp and show that the closed loop voltage gain is given by $A_{vf} = \frac{A_v}{(1+A_v\beta)}$.

A_v - open loop voltage gain of opamp.

β - feedback factor.

Soln:

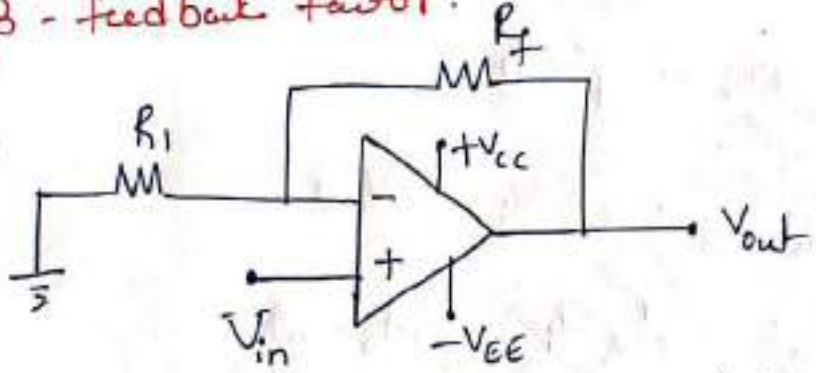


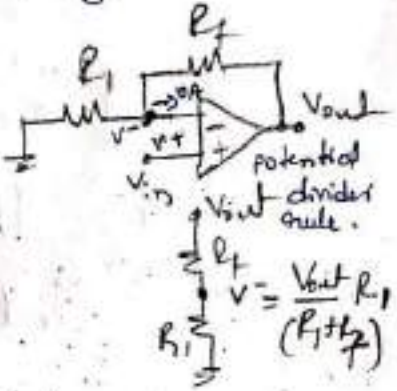
fig. Non-Inverting amplifier.

W.K.T Gain of the Non-inverting amplifier is

$$A_{vf} = \frac{V_{out}}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right) \longleftarrow (1)$$

Eqn (1) was derived assuming that open loop gain $A_v = \infty$.

for finite value of A_v, the differential voltage amplified by the op-amp is.



$$V_d = V^+ - V^-$$

$$V_d = V_{in} - \frac{V_{out}}{(R_1+R_f)} \cdot R_1$$

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where $\beta = \frac{R_1}{R_1+R_f}$ feedback factor.

$$\therefore \boxed{V_d = V_i - \beta V_{out}} \leftarrow (2)$$

W.K.T $V_{out} = A_V \cdot V_d \leftarrow (3)$

Eq" (2) in eq" (3)

$$V_{out} = A_V (V_i - \beta V_{out})$$

$$V_{out} = A_V V_i - \beta A_V V_{out}$$

$$V_{out} + \beta A_V V_{out} = A_V \cdot V_i$$

$$V_{out}(1+\beta A_V) = A_V$$

$$\boxed{A_{Vf} = \frac{V_{out}}{V_{in}} = \frac{A_V}{(1+\beta A_V)}}$$

A_V ← open loop gain

A_{Vf} ← gain with feedback

Note:- thus By going -ve feedback, Gain with feedback will be reduced by a factor of $(1+\beta A_V)$

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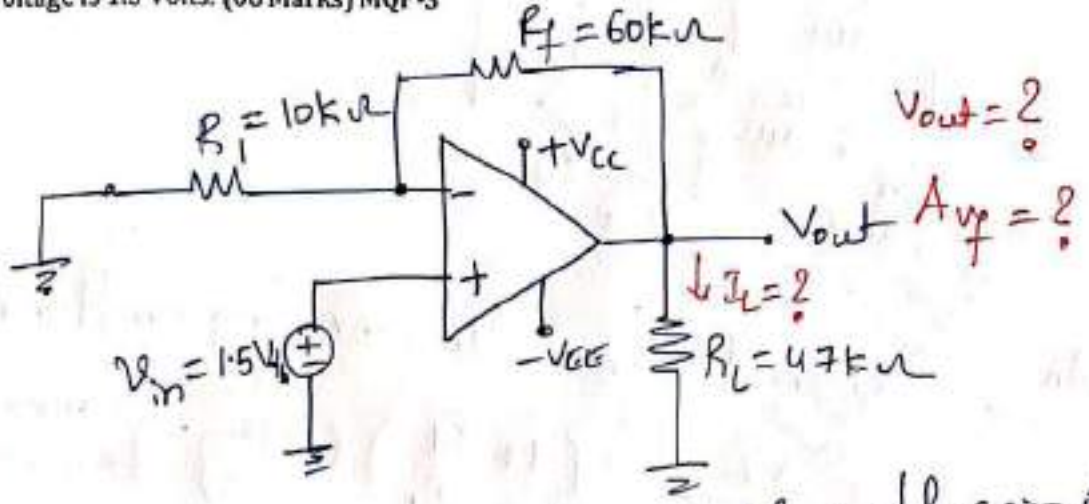
A non inverting amplifier circuit has an input resistance of 10KΩ and feedback resistance 60 KΩ with load resistance of 47KΩ. Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is 1.5 Volts. (08 Marks) MQP-3

Soln:-



Given it is an Non-inverting amplifier. the gain

$$A_{vf} = \left(1 + \frac{R_f}{R_1}\right)$$

$$= \left(1 + \frac{60k}{10k}\right) = 1 + \frac{60}{10} = (1+6) = 7$$

i. Voltage gain with feedback $\boxed{A_{vf} = \frac{V_{out}}{V_{in}} = 7}$

ii. The output voltage $V_{out} = A_{vf} \cdot V_{in}$

$$\Rightarrow V_{out} = (7)(1.5) = 10.5 \text{ volts}$$

$\boxed{V_{out} = 10.5 \text{ volts}}$

iii. Load Current $I_L = \frac{V_{out}}{R_L} = \frac{10.5}{47k} = 0.2234 mA$

$\boxed{I_L = 0.2234 mA}$

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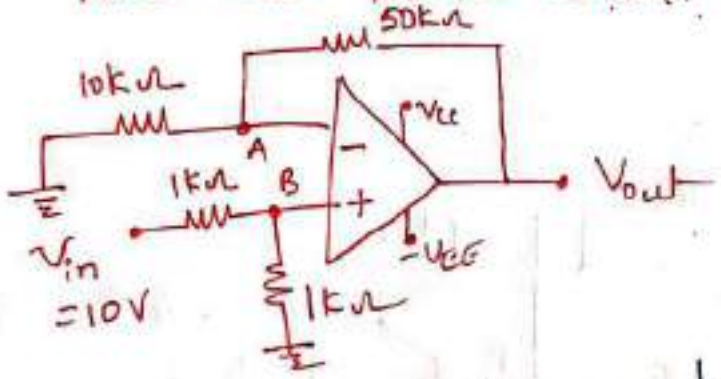
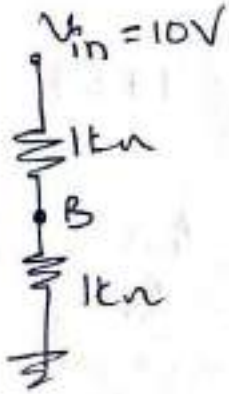
Question. Find V_{out} for the circuit shown in the fig.



Soln:- Given it is an Non-inverting amplifier

$$V_{out} = \left(1 + \frac{R_f}{R_1}\right) \cdot (\text{voltage at noninverting terminal})$$

ie $$\boxed{V_{out} = \left(1 + \frac{R_f}{R_1}\right) \cdot V_B}$$



using VDR

$$V_B = \frac{V_{in}}{(1K+1K)}(1K) = \frac{V_{in}}{2} = 5 \text{ volts}$$

$$\boxed{V_B = 5 \text{ volts}}$$

$$\therefore V_{out} = \left(1 + \frac{50K}{10K}\right)(5)$$

$$V_{out} = (1+5)(5) = 6 \times 5$$

$$\boxed{V_{out} = 30 \text{ volts}}$$

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Q.6 :- **Inverting Amplifier:-**

Explain the operation of an Op-AMP as inverting amplifier with neat diagram and waveforms. /(06 Marks) Dec 2019-Jan 2020./ MQP-1/MQP-3

Soln:- * An amplifier which provides a phase shift of 180° between input and output is called inverting amplifier.

* The basic circuit diagram of an inverting amplifier using op-amp is shown in fig a.

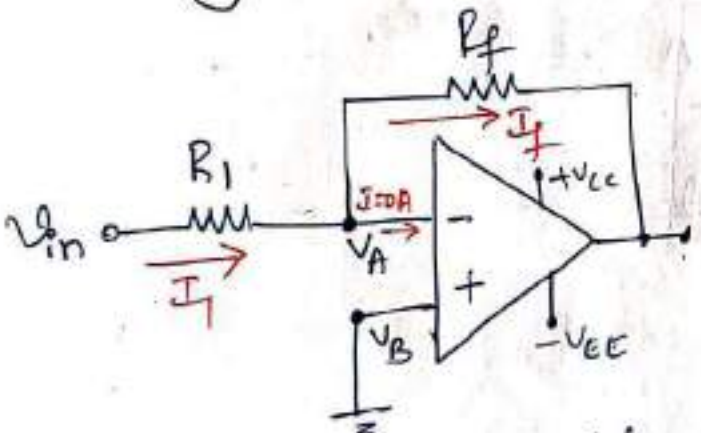

fig a:- inverting amplifier

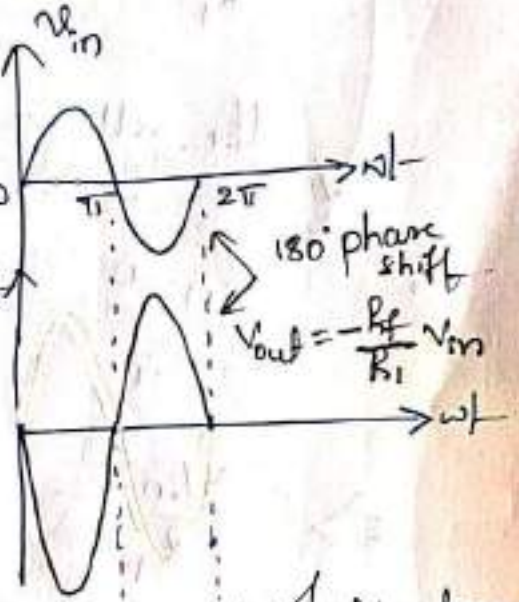

fig b:- i/p and o/p waveforms of inverting opamp.

* The potential at node B is Zero due to virtual ground Concept the potential at node A is also Zero.

$$\therefore \boxed{V_A = V_B = 0} \text{ volt.}$$

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* The opamp input Current is always Zero hence entire Current I passes through the Resistance R_f.

KCL at node A.

ie incoming Current equal to outgoing Current.

$$I_1 = I_f$$

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_{out}}{R_f}$$

the voltage @ node A ie $V_A = 0$.

$$\therefore \frac{V_{in} - 0}{R_1} = \frac{0 - V_{out}}{R_f}$$

$$\Rightarrow \frac{V_{in}}{R_1} = -\frac{V_{out}}{R_f}$$

Gain with feedback $\boxed{A_{vf} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1}}$

$$V_{out} = \left(-\frac{R_f}{R_1}\right) V_{in}$$

where (R_f/R_1) is closed loop gain of opamp and -ve Sign indicates that output Signal is 180° phase shift of input Signal.

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SUMMING (or) ADDER Amplifier :-

Question: Derive an Expression for the output voltage of an inverting Summer. (06 Marks) MQP-3.

Soln:- When more than one input signal is applied to the Inv (or) Non-Inv amplifier, the output contains addition of the applied input signals. Hence it is called Summer (or) adder amplifier circuit.

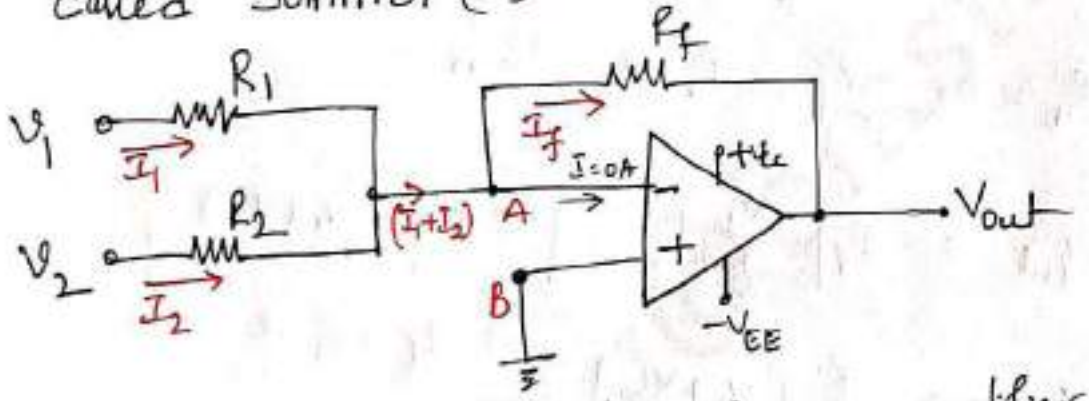

fig:- Inverting Summing amplifier

from the concept of Virtual ground $V_A = V_B = 0$ volts.

KCL at node A.

$$I_1 + I_2 = I_f$$ (i.e Incoming Currents is equal to Outgoing Currents)

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = \frac{V_A - V_{out}}{R_f} \leftarrow (1)$$

the potential at node A, i.e $V_A = 0$ volts

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$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{-V_{out}}{R_f}$$

$$\Rightarrow V_{out} = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2$$

$$V_{out} = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right]$$

if $R_1 = R_2 = R\,\Omega$, then

$$\boxed{V_{out} = -R_f \left[\frac{V_1}{R} + \frac{V_2}{R} \right] = -\frac{R_f}{R}(V_1 + V_2)}$$

if $R_f = R\,\Omega$

then $$V_{out} = -\frac{R}{R}[V_1 + V_2]$$

$$\boxed{V_{out} = -(V_1 + V_2)}$$

Due to the negative sign of the sum at the output it is called inverting Summing amplifier. it shows that there is phase inversion.

note:- Average ckt:- In the above ckt if $R_1 = R_2 = R\,\Omega$ and $R_f = R/2$ then output $V_{out} = -\left(\frac{V_1 + V_2}{2}\right)$ i.e average of the inputs.

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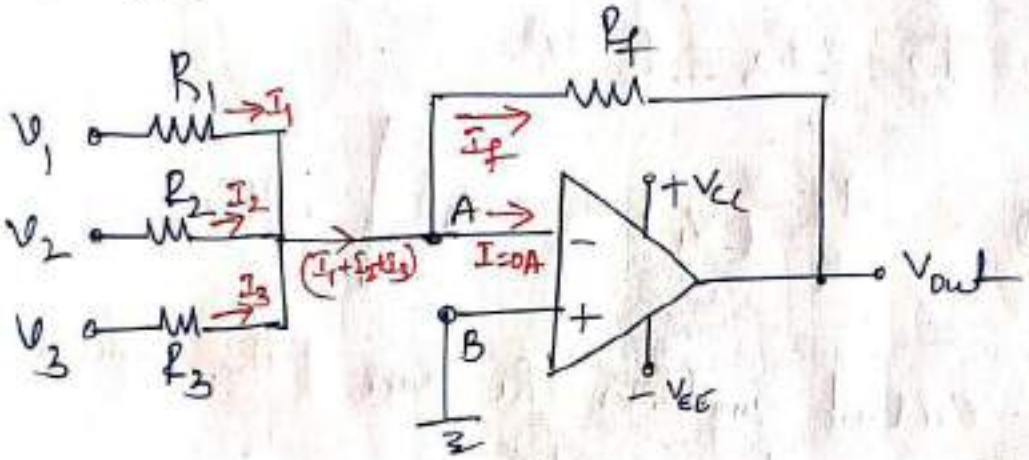
Draw the three input inverting summer circuit and derive an expression for its output voltage. (8 Marks) MQP-1

Soln:- * In this Circuit, all the input Signals to be added are applied to the inverting input terminal of the op-amp.

* The Circuit with three inputs is shown in the figa.



figa:- three input inverting Summer.

* From the Concept of Virtual ground $V_A = V_B = 0$ volt,

KCL at node A

ie $I_1 + I_2 + I_3 = I_f$ (incoming Current is equal to outgoing Current)

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_{out}}{R_f} \leftarrow (1)$$

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the potential at node A i.e $V_A = 0$ volts

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{0 - V_{out}}{R_f}$$

$$\Rightarrow V_{out} = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

if $R_1 = R_2 = R_3 = R\ \Omega$

then $\boxed{V_{out} = -\frac{R_f}{R}(V_1 + V_2 + V_3)}$ volts,

Thus the circuit amplifies the sum of the inputs in an inverting mode.

if $R_f = R\ \Omega$, then

$$\boxed{V_{out} = -[V_1 + V_2 + V_3]}$$ volts.

Due to the negative sign there exists phase difference of 180° between input and output hence circuit is called inverting Summing Amplifier.

Note:- if $R_1 = R_2 = R_3 = R\ \Omega$ and $R_f = R/3$ then o/p $V_{out} = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$ ie avg of the inputs.

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Design an Op-Amp circuit to obtain output expression as $V_0=-[V_1+3V_2+5V_3]$. (06 Marks) June-July 2019.

Soln:- W.K.t the output of three input inverting Summer is

$$V_{out} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \leftarrow (1)$$

given $V_{out} = -[V_1 + 3V_2 + 5V_3] \leftarrow (2)$

By comparing eq^n (1) & eq^n (2)

$$\frac{R_f}{R_1} = 1 \quad , \quad \frac{R_f}{R_2} = 3 \quad \frac{R_f}{R_3} = 5$$

$\boxed{R_f = R_1}$ $\quad R_2 = \frac{R_f}{3}$, $R_3 = \frac{R_f}{5}$

choose $R_f = 15k\Omega$, $\quad = \frac{15k}{3}$ $\quad R_f = 15k\Omega$

$\Rightarrow \boxed{R_1 = 15k\Omega}$ $\quad \boxed{R_2 = 5k\Omega}$ $\quad \therefore R_3 = \frac{15k}{5}$

$\boxed{R_3 = 3k\Omega}$

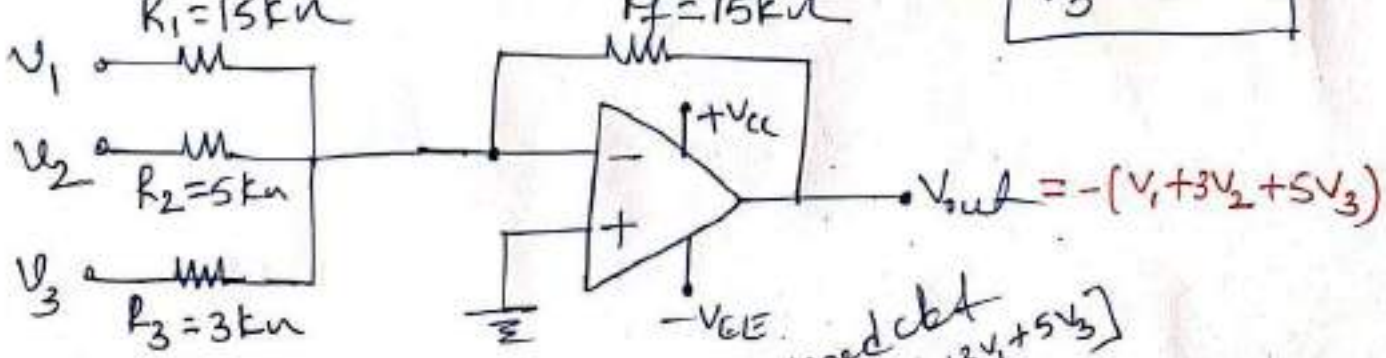

fig a. The designed ckt for $V_{out} = -[V_1+3V_1+5V_3]$

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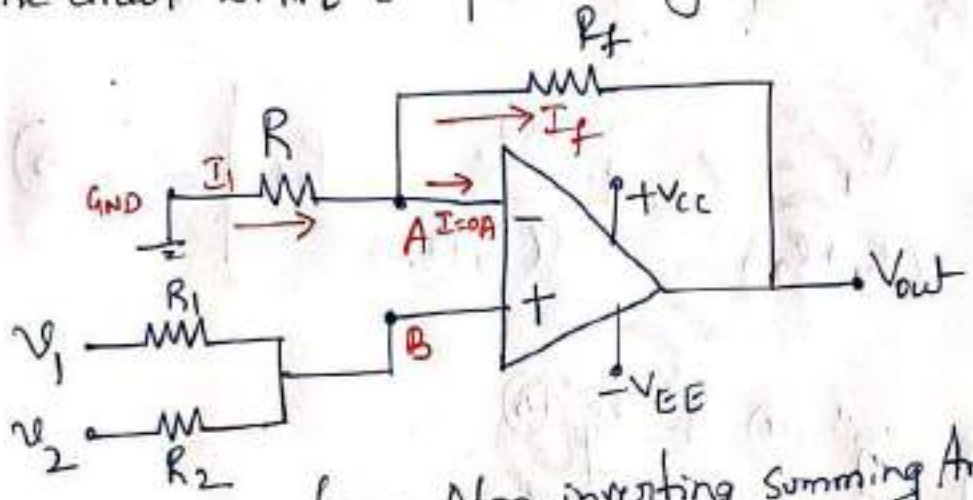
Non-Inverting Summing Amplifier:-

* A summer circuit that gives amplification of non-inverted sum of the input signals is called "non-inverting Summing amplifier."

* The circuit with two input voltages is shown in the figa.



figa:- Non-inverting Summing Amplifier.

* from virtual ground Concept.

$$V_A = V_B.$$

V_A using VDR $\Rightarrow V_A = \dfrac{V_{out}}{(R+R_f)} \cdot R \leftarrow (a)$

voltage V_B. using Superposition principle.

$V_{B_1} = \dfrac{v_1}{(R_1+R_2)} \cdot R_2$; when v_1 acting alone by setting [$v_2 = 0$ volts]

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$$V_{B_2} = \frac{V_2}{(R_1+R_2)} \cdot R_1$$ (when v_2 acting alone by setting $v_1 = 0$ volts]

$$V_B = V_{B_1} + V_{B_2}$$: (when v_1 & v_2 acting simultaneously)

$$\boxed{V_B = \frac{v_1}{(R_1+R_2)} \cdot R_2 + \frac{v_2}{(R_1+R_2)} \cdot R_1} \leftarrow (6)$$

Equating eq^n (a) & eq^n (b)

i.e $V_A = V_B$.

$$\frac{V_{out}}{(R+R_f)} \cdot R = \frac{v_1}{(R_1+R_2)} \cdot R_2 + \frac{v_2}{(R_1+R_2)} \cdot R_1$$

$$\boxed{V_{out} = \frac{R_2(R+R_f)}{R(R_1+R_2)} v_1 + \frac{R_1(R+R_f)}{R(R_1+R_2)} \cdot v_2} \text{ volts.}$$

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* if the two resistances R_1 and R_2 are selected Equal ie $R_1 = R_2 = R$, then

$$V_{out} = \frac{(R+R_f)}{2R}\left[V_1 + V_2\right] \quad \leftarrow @$$

* Thus Circuit amplifies the addition of the two inputs.

if $R_1 = R_2 = R_f = R$ ie

then $V_{out} = (V_1 + V_2)$

As there is no phase difference between input and output, it is called non-inverting Summer amplifier.

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Design an adder circuit using Op-Amp to obtain output Voltage as $V_0 = -[2V_1+3V_2+5V_3]$ assume R_f =10KΩ (06 Marks) Dec 2019-Jan 2020./ MQP-1/MQP-2.

Soln: The output of inverting adder is

$$V_{out} = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right] \leftarrow (1)$$

given $$V_{out} = -[2V_1 + 3V_2 + 5V_3] \leftarrow (2)$$

[Comparing eq^n (1) and eq^n (2)

$$\frac{R_f}{R_1} = 2, \quad \frac{R_f}{R_2} = 3, \quad \frac{R_f}{R_3} = 5$$

given $R_f = 10k\Omega$ (choose)

$R_1 = \frac{R_f}{2} = \frac{10k}{2}$ | $R_2 = \frac{R_f}{3} = \frac{10k}{3}$ | $R_3 = \frac{R_f}{5} = \frac{10k}{5}$

$\boxed{R_1 = 5k\Omega}$ | $\boxed{R_2 = 3.33k\Omega}$ | $\boxed{R_3 = 2k\Omega}$

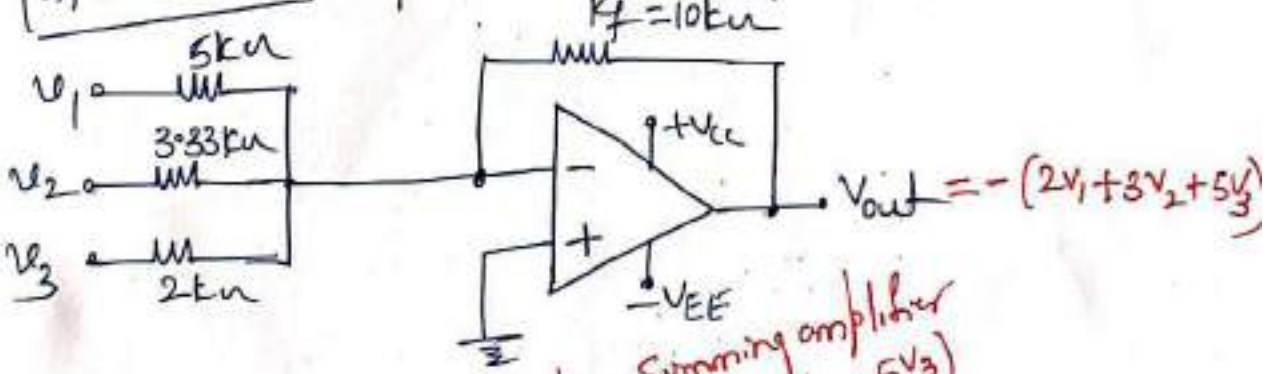

fig:- inverting Summing amplifier for $V_{out} = -(2V_1+3V_2+5V_3)$

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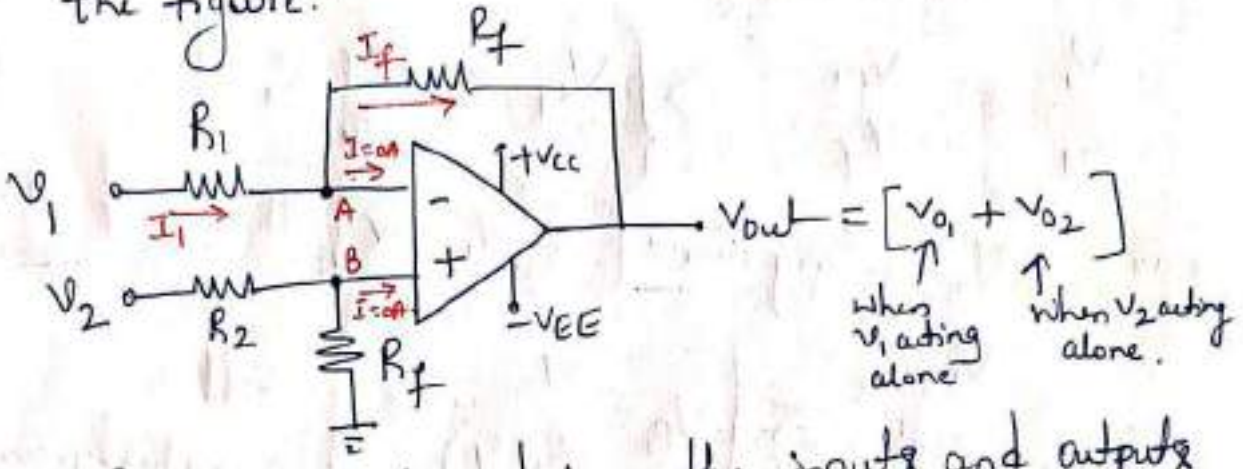
Difference Amplifier (or) Subtractor

Explain op-amp as a subtractor with neat circuit diagram. **(08 Marks) Dec 2018-Jan 2019.**

* The Circuit diagram of opamp Subtractor is shown in the figure.



* To find the relation between the inputs and outputs use Superposition principle. [i.e considering one source(i/p) acting at a time]

Consi
i.e Let V_{o1} be the output, with the input V_1 acting alone (i.e $V_2 = 0$).

if $V_2 = 0V$ then potential at node B is equal to zero. bcz $V_B = \left(\frac{V_2}{R_1+R_f}\right).R_f$ By VDR

$V_2 = 0V$ then $\boxed{V_B = 0}$ volts

from Virtual ground Concept $V_A = V_B$

$\therefore \boxed{V_A = 0}$ volts (Sinc $V_B = 0$ volts)

KCL at node A. $I_1 = I_f$ (ie incoming Current equal to outgoing Current)

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$$\frac{v_1 - V_A}{R_1} = \frac{V_A - V_{01}}{R_f}$$

$V_A = 0$ volt's

$$\frac{v_1}{R_1} = \frac{-V_{01}}{R_f} \Rightarrow \boxed{V_{01} = -\frac{R_f}{R_1} v_1} \leftarrow (a)$$

Case ii: V_2 acting alone [i.e $v_1 = 0$V] the corresponding o/p voltage V_{02}.

By using VDR $\Rightarrow$ $\boxed{V_B = \frac{V_2}{(R_1+R_f)} \cdot R_f}$

By virtual ground concept $\boxed{V_A = V_B}$

KCL at node A : i.e $I_1 = I_f$

$$\frac{0 - V_A}{R_1} = \frac{V_A - V_{02}}{R_f}$$

$$\therefore V_{02} = \left(1 + \frac{R_f}{R_1}\right) \cdot V_A$$

$$V_A = V_B = \frac{V_2}{(R_1+R_f)} R_f$$

$$\therefore V_{02} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_f}{R_1+R_f}\right) V_2$$

$$V_{02} = \frac{(R_1+R_f)}{R_1} \cdot \frac{(R_f)}{(R_1+R_f)} V_2$$

$$\boxed{V_{02} = \frac{R_f}{R_1} V_2} \leftarrow (b)$$

UB.

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the total output voltage (V_{out}) by considering both inputs acting at a time.

i.e $V_{out} = V_{o_1} + V_{o_2}$

$$V_{out} = -\frac{R_f}{R_1} v_1 + \frac{R_f}{R_1} v_2$$

$$\boxed{V_{out} = \frac{R_f}{R_1}(v_2 - v_1)}$$

Thus o/p voltage is proportional to the difference b/w the two input voltages.

if $R_f = R_1 = R\ \Omega$

then $\boxed{V_{out} = (v_2 - v_1)}$ ⇐ o/p of Subtractor.

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Explain how Op-amp can be used as i) Integrator and ii) Voltage follower. **(08 Marks) June-July 2019. /(08 Marks) Dec 2019-Jan 2020./ MQP-2/MQP-3**

ii. Voltage follower:-

* A Circuit in which the output voltage follows the input voltage is called voltage follower circuit.
* The voltage follower circuit using op-amp is shown in fig.

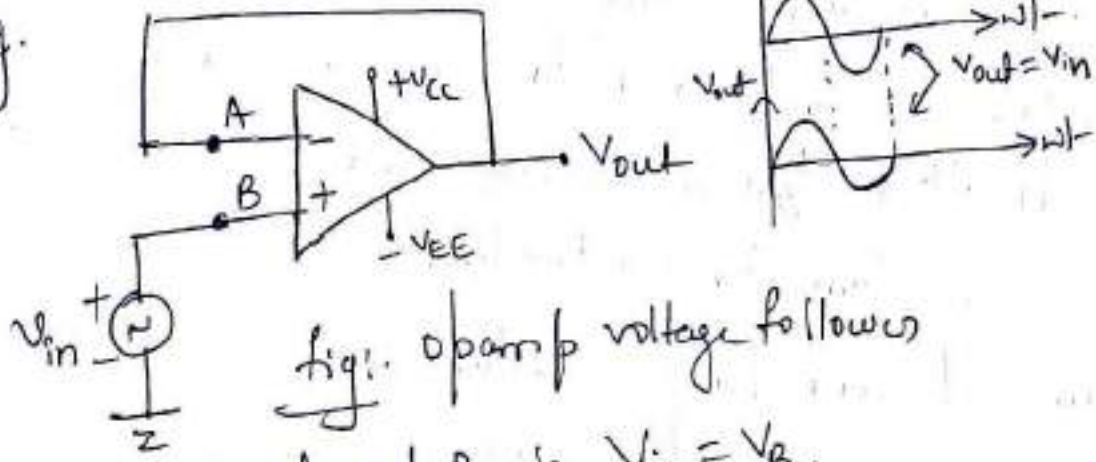

fig: opamp voltage follower

* The potential at node B is $V_{in} = V_B$.
* concept of virtual ground $\boxed{V_A = V_B = V_{in}}$
* node A is directly connected to the output node

hence $\boxed{V_{out} = V_A = V_{in}} \Rightarrow \frac{V_{out}}{V_{in}} = 1$

$$\boxed{A_{vf} = \frac{V_{out}}{V_{in}} = 1}$$

* the gain of the voltage follower ckt is one. hence it is also called Unity gain ckt.

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* Voltage follower circuit is also called as Source follower, unity gain Amplifier, Buffer amplifier, (or) isolation amplifier.

Advantages of Voltage follower :-

i. Very large input impedance of the order MΩ.

ii. Low output impedance almost Zero.
Hence it can be used to connect high impedance Source to a Low impedance Load, as a buffer. This Eliminates the loading Effect.

iii. It has Large Bandwidth.

iv. the output follows the input Exactly without a phase shift.

"Tell me and I Forget, Show me and I remember, Let me do and I Understand"

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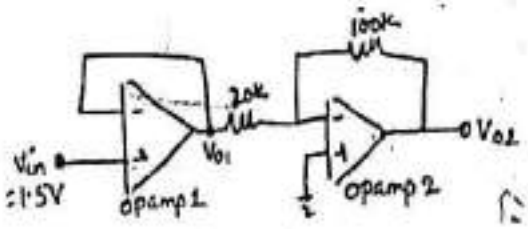
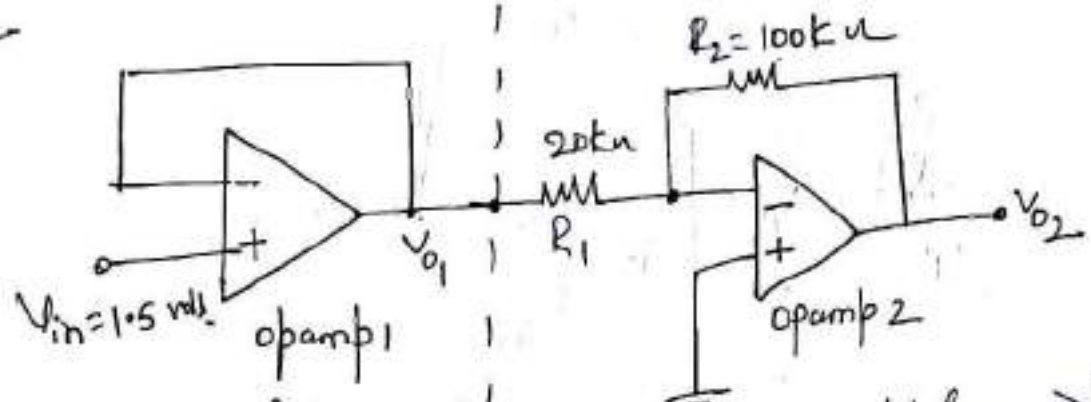
For an op-amp circuit shown in fig. Find the output Vo1 and Vo2. Also write the function of each op-amp used. **(06 Marks) Dec 2018-Jan 2019 /MQP-1**



Soln:-



← voltage follower → | ← inverting amplifier →

Since opamp-1 ckt is a voltage follower ckt.

$$\therefore \boxed{V_{o_1} = V_{in} = 1.5 \text{ volts}}$$

opamp-2 ckt is an inverting amplifier

$$V_{o_2} = -\frac{R_f}{R_1} \cdot V_g = \frac{-100k}{20k}(1.5)$$

$$= -5(1.5)$$

$$\boxed{V_{o_2} = -7.5 \text{ volts}}$$

function:-
opamp1 ckt:- voltage follower
opamp2 ckt:- inverting amplifier.

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OPAMP INTEGRATOR

* In an Integrator Circuit, the output voltage is the integration of the input voltage.
* the op-amp integrator Circuit in shown in fig.

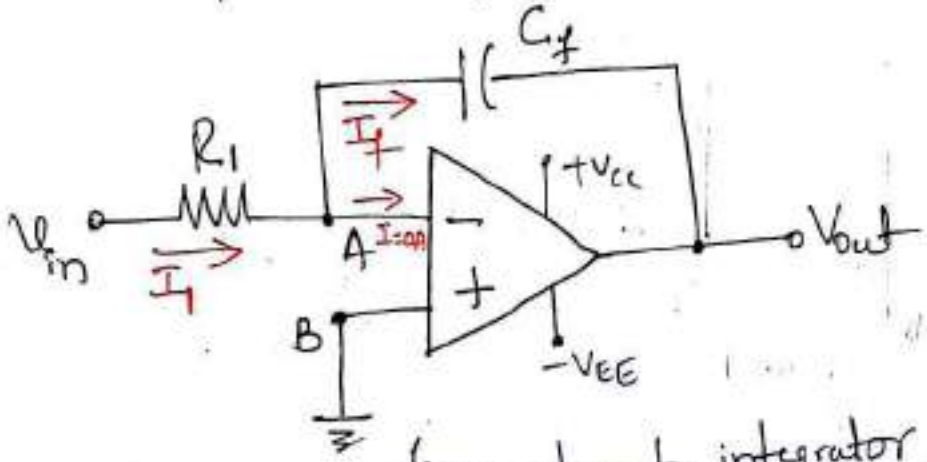


fig a:- op-amp integrator

* node B is grounded. from virtual ground concept

$$V_B = V_A = 0 \text{ volts.}$$

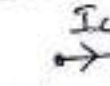
* KCL at node A

$$I_1 = I_f \quad (\text{ie incoming current is equal to outgoing current})$$

$$\frac{V_{in} - V_A}{R_1} = C_f \frac{d[V_A - V_{out}]}{dt}$$

$$\Rightarrow V_A = 0 \text{ volts}$$

Note:- v-i relationship in capacitor.



$$V_c = \frac{1}{C}\int i_c\, dt$$

(or)

$$i_c = C\frac{dV_c}{dt}$$

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$$\frac{V_{in}}{R_1} = C_f \frac{d}{dt}(-V_{out})$$

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_{out}}{dt}$$

$$\frac{dV_{out}}{dt} = -\frac{1}{R_1 C_f} \cdot V_{in}$$

integrating on both sides w.r.t t

$$\boxed{V_{out} = -\frac{1}{R_1 C_f} \int_0^t v_{in}\, dt \text{ volts}} \leftarrow (a)$$

the above eq^n is valid by assuming initial voltage of capacitor is Zero. i.e $V_c(0^-) = 0$ volts

* from eq^n (a) the output is $\frac{-1}{R_1 C_f}$ times the integral of the input and $R_1 C_f$ is called time constant of the integrator.

* V_i (i/p Signal)	$V_{out} = \int v_i dt$ (o/p Signal)
Sin	Cos
step	ramp
Square	triangular

Applications of integrator ckt :-

* In analog Computers.
* In solving differential equations.
* In ramp wave generators.
* In Analog to digital conversion.
* In various wave shaping ckts.

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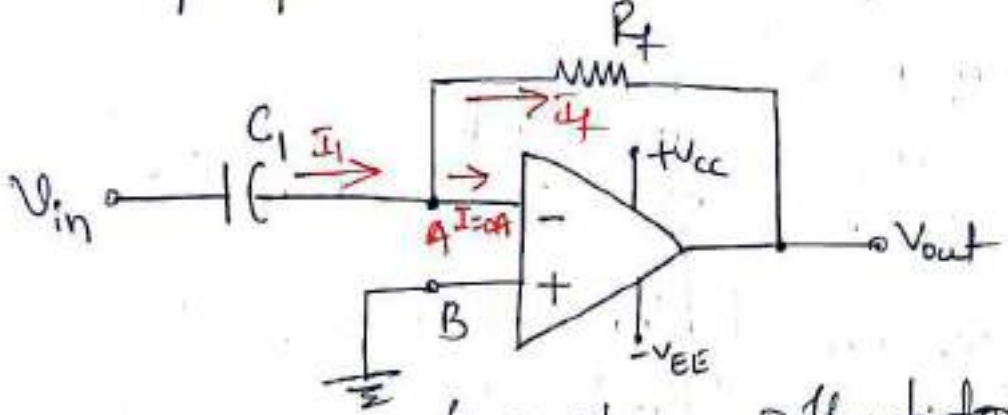
Op-Amp Differentiator :-

Explain how op-amp can be used as differentiator. **(06 Marks) June-July 2019./MQP-1**

Soln:- * The Circuit which produces the differentiation of the input voltage at its output is called differentiator.

* The op-amp differentiator circuit is shown in figa.



figa:- Op-amp Differentiator.

* the node B is grounded $\therefore V_B = 0$.

from Virtual ground Concept $V_A = V_B = 0$ volts.

* KCL at node A.

$$I_1 = I_f$$ [ie incoming current is equal to outgoing current]

$$\therefore C_1 \frac{d}{dt}[V_{in} - V_A] = \frac{V_A - V_{out}}{R_f}$$

using $V_A = 0$ volts.

$i \rightarrow$ + v −

$v_c = \frac{1}{C}\int i\,dt$

$i_c = C\frac{dv_c}{dt}$

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$$C_1 \frac{dv_{in}}{dt} = -\frac{V_{out}}{R_f}$$

$$\Rightarrow \boxed{V_{out} = -C_1 R_f \frac{dv_{in}}{dt}} \text{ volts}$$

* The equation shows that the output is C_1R_f times the differentiation of the input and product C_1R_f is called time constant of the differentiator.

* The negative sign indicates that there is a phase shift of 180° b/w input and output.

*

i/p Signal v_i	o/p signal $V_{out} = -d/dt(v_{in})$
Sine	- Cosine
Step	impulse
Square	impulse train.

* Applications of differentiator :-

→ In the wavechaping circuit to detect the high frequency components in the input signal. (HPF)

→ As a rate-of-change detector in the FM demodulators.

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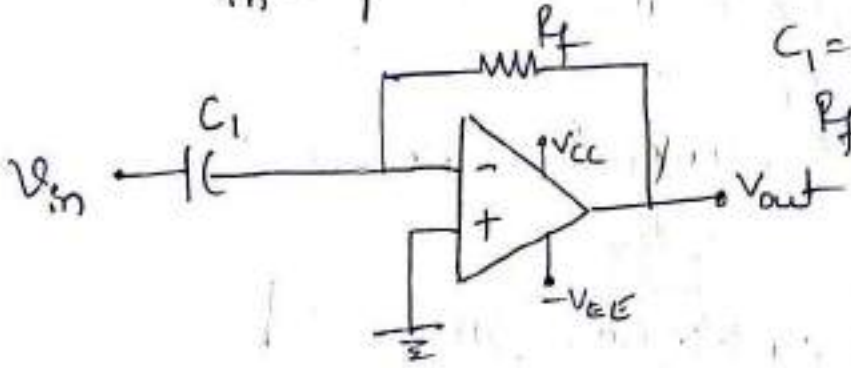
The input to the basic differentiator circuit is a sinusoidal voltage of peak value of 10mV and frequency 1.5 KHz. Find the output if, R_f=100KΩ and C_1=1μF. **(6 Marks) MQP-3**

Soln:

$V_p = 10mV$, $\omega = 2\pi f$ rad/sec

$f = 1.5kHz$.

$V_{in} = V_p \sin\omega t$



$C_1 = 1\mu F$

$R_f = 100k\Omega$.

the output of differentiator circuit is

$$V_{out} = -C_1 R_f \frac{d(V_{in})}{dt}$$

given $V_{in} = V_p \sin(\omega t)$

$$V_{out} = -C_1 R_f \, d/dt \, [V_p \sin\omega t]$$

$$= -C_1 R_f V_p \times \cos\omega t \times \omega$$

$$\boxed{V_{out} = -C_1 R_f V_p \omega \cos\omega t} \text{ volts.}$$

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$$V_{out} = -C_1 V_p R_f \omega \cos \omega t$$

$$= -C_1 V_p R_f \times 2\pi f \times \cos[2\pi f t]$$

$$= 10\times10^{-3} \times -1\times10^{-6} \times 100\times10^{3} \times 2\pi \times 1.5\times10^{3} \cos[2\pi \times 1.5\times10^{3} t]$$

$$V_{out} = -9.42477 \cos[3\pi \times 10^{3} t]$$

$$\boxed{V_{out} = -9.42477 \cos[9424.77 t]} \text{ volts.}$$

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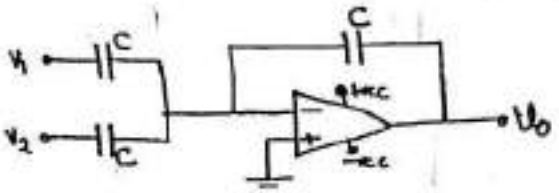
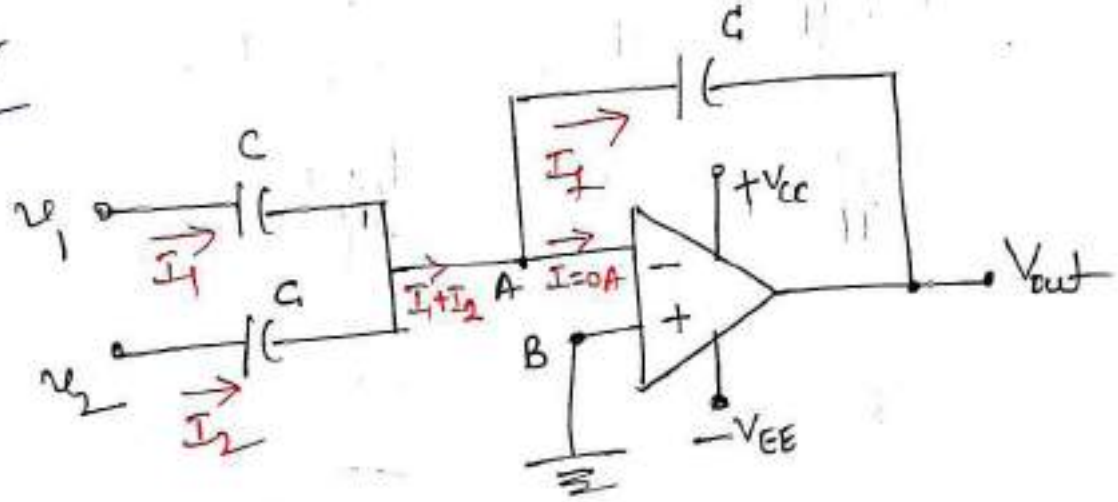
Find the output of the Op-amp circuit shown in Fig. below. **(08 Marks) June-July 2019**



Soln:-



potential at node B i.e $V_B = 0$ volts.

from virtual ground concept $V_A = V_B = 0$ volts.

kcl at node A.

$$I_1 + I_2 = I_f$$ (i.e incoming current is equal to outgoing current).

$$C\frac{d(V_1 - V_A)}{dt} + C\frac{d(V_2 - V_A)}{dt} = C\frac{d}{dt}(V_A - V_{out})$$

$$V_A = 0 \text{ volts.}$$

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$$C\frac{dv_1}{dt} + C\frac{dv_2}{dt} = -C\frac{dV_{out}}{dt}$$

$$C\left[\frac{dv_1}{dt} + \frac{dv_2}{dt}\right] = -C\frac{dV_{out}}{dt}$$

$$\frac{d}{dt}(v_1 + v_2) = \frac{d}{dt}(-V_{out})$$

$$\Rightarrow \quad v_1 + v_2 = -V_{out}$$

$$\therefore \boxed{V_{out} = -(v_1 + v_2)}$$

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Opamp Comparator:

- A **comparator** is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input, and produce either a high or a low output voltage, depending on which input is higher.
- It produces output voltage which is either positive saturation voltage (+ V_{sat}) or negative saturation voltage (– V_{sat}).
- As comparator output has two voltage levels, either high or low, it is not linearly proportional to input voltage.
- The op-amp is used in a open loop configuration for a comparator.
- There are two types of comparator circuits which are,
  1. Non-inverting comparator and
  2. Inverting comparator

Basic Non-inverting Comparator

➢ ***Explain the operation of an op-amp as a basic non-inverting comparator.***

- The **basic non-inverting comparator** is shown in the Fig.

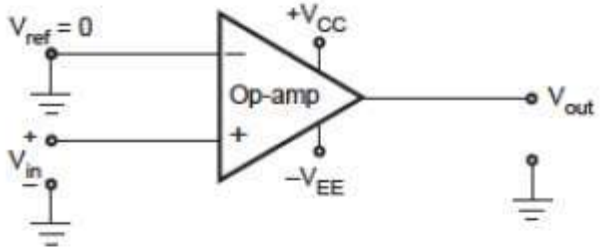

Fig. Basic non-inverting comparator

- In this comparator, the input voltage is applied to the non-inverting terminal and no reference voltage is applied to other terminal.
- So inverting terminal is grounded.

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- The input voltage is denoted as V_{in} while the voltage applied to other terminal with which V_{in} is compared is denoted as V_{ref}.
- In the basic comparator, $V_{ref} = 0$ V.
- In the non-inverting comparator, if V_{in} is greater than V_{ref} then output is $+ V_{sat}$ i.e. almost equal to $+ V_{CC}$.
- While if V_{in} is less than V_{ref} then output is $- V_{sat}$ i.e. almost equal to $- V_{EE}$.
- Thus for the Fig. , as $V_{ref} = 0$ V when V_{in} is positive then $V_o = + V_{sat}$ while when V_{in} is negative then $V_o = - V_{sat}$.
- This is because, as open loop gain op-amp (A_{OL}) is very very high even for very small V_{in} the op-amp output saturates.

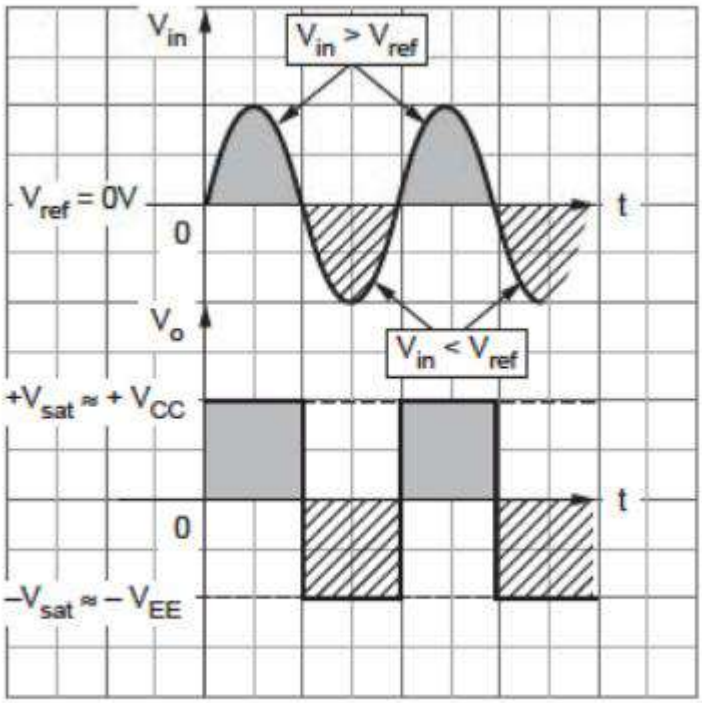

Fig. Waveforms of a basic non-inverting comparator

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- The input and output waveforms for a basic non-inverting comparator, for sinusoidal input are shown in the Fig.
- By applying any voltage other than zero to the inverting input terminal, the tripping of comparator can be changed as per the requirements. In such a case V_{in} is compared with the reference voltage V_{ref} applied to the inverting terminal.
- If $V_{in} > V_{ref}$ then the output is $+ V_{sat}$ while if $V_{in} < V_{ref}$ then the output is at $- V_{sat}$.

- For positive V_{ref}, the waveforms are shown in the Fig. (a) while for negative V_{ref} the waveforms are shown in the Fig. (b).

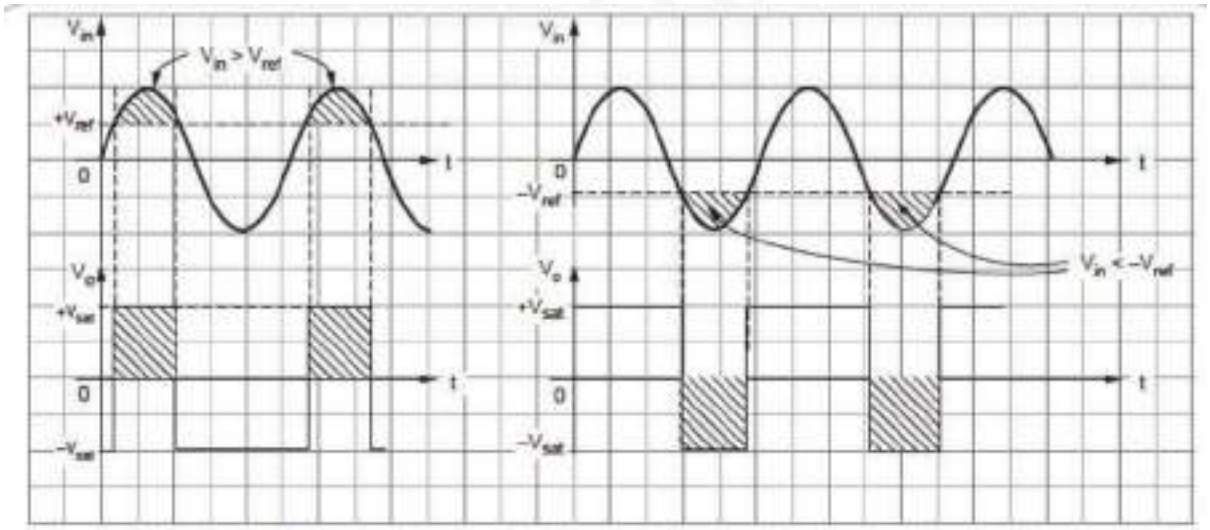

Fig. Input and output waveforms

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Basic Inverting Comparator

➢ ***Explain the operation of an op-amp as a basic inverting comparator.***

- The Fig. shows inverting comparator in which the reference voltage V_{ref} is applied to the non-inverting (+) input and signal voltage (V_{in}) is applied to the inverting (–) input of the op-amp.
- The V_{ref} = 0 V as non-inverting terminal is grounded.

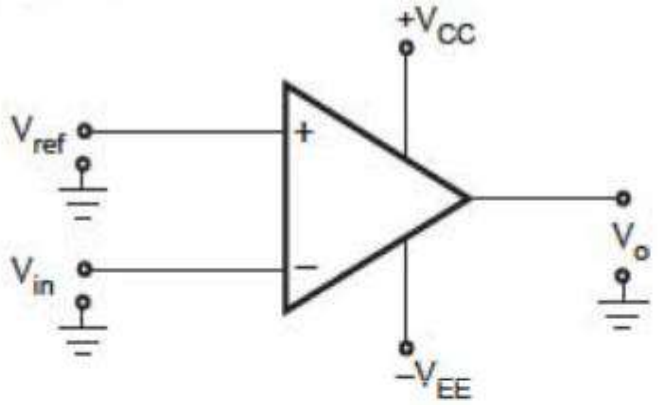

Fig. Basic inverting comparator

- When V_{in} is less than V_{ref}, the output voltage V_o is at $+V_{sat}$ ($\cong +V_{CC}$) because the voltage at the inverting input (–) is less than that at the non-inverting (+) input.
- On the other hand, when V_{in} is greater than V_{ref}, V_o goes to $-V_{sat}$ ($\cong -V_{EE}$).

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- The V_{ref} can be set other than zero by using a battery and potential divider as per the requirement.
- The Fig. shows the input and output waveforms for inverting comparator with positive and negative values of V_{ref}.

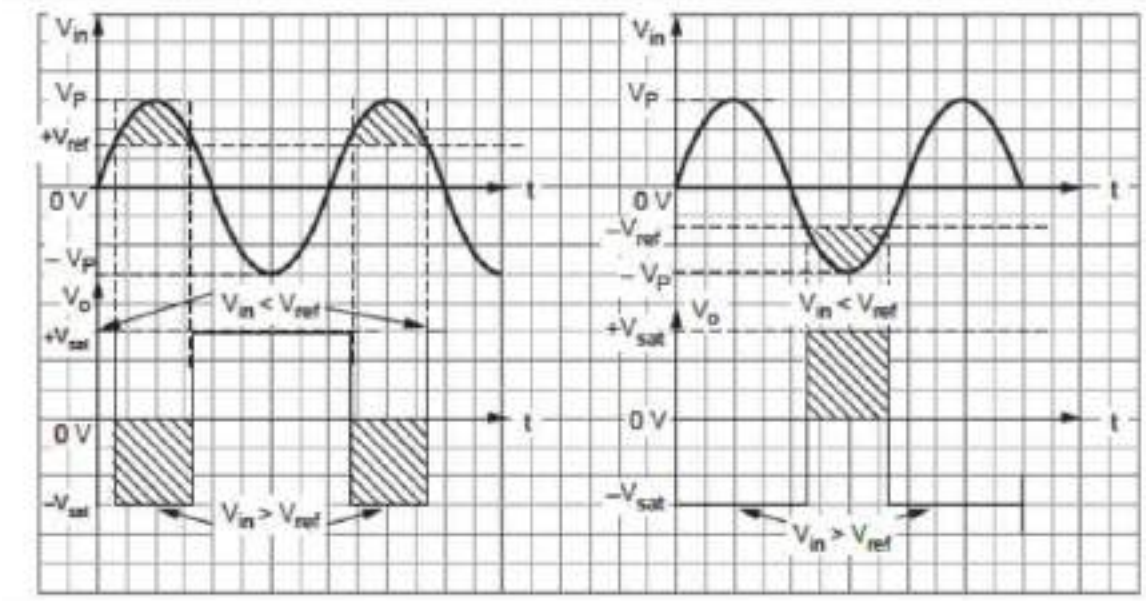

Fig. Input and output waveforms for inverting comparator

List the applications of comparator

- The various applications of comparator are,
  1. Zero crossing detector
  2. Level detector
  3. Window detector
  4. Duty cycle controller
  5. Pulse generator

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Miscellaneous Topic:

➢ ***Explain the function of differential amplifier.***

VTU : Mar.-2000, Marks 4

- The ideal op-amp is basically an amplifier which amplifies the difference between the two input signals. Hence it is called the **differential amplifier** or **difference amplifier.**

- Consider an ideal differential amplifier shown in the Fig.

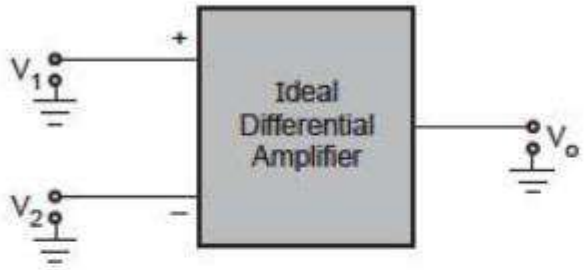

Fig. Ideal differential amplifier

- V_1 and V_2 are the two input signals while V_o is the single ended output. Each signal is measured with respect to the ground.
- In an ideal differential amplifier, the output voltage V_o is proportional to the difference between the two input signals. Hence we can write,

$$V_o \propto (V_1 - V_2)$$

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Differential Gain A_d

➢ ***Define the differential gain of a basic differential amplifier.***

➢ ***What is difference voltage ? How differential gain is expressed in decibels ?***

$V_o = A_d (V_1 - V_2)$

where A_d is the constant of proportionality.

- The A_d is the gain with which differential amplifier amplifies the difference between two input signals. Hence it is called **differential gain. Thus, A_d = Differential gain.**
- The difference between the two inputs $(V_1 - V_2)$ is generally called **difference voltage** and denoted as V_d.

$$\therefore \quad V_o = A_d V_d$$

- Hence the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d}$$

- Generally the differential gain is expressed in its decibel (dB) value as,

$$A_d = 20 \text{ Log}_{10} (A_d) \text{ in dB}$$

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Miscellaneous Problems

Problem on Slew rate:

An op - amp has a slew rate of 0.5 V/µsec.
i) What is the maximum undistorted sine wave which can be produced at a frequency of 6.631 kHz ?
ii) What is the maximum frequency of the sine wave that op-amp can produce at the output without distortion with peak value of 7 volts ?

Sol. :

i) $f = 6.631$ kHz, $S = 0.5$ V/µsec

$$S = \frac{0.5}{10^{-6}} \text{ V/sec} = 0.5\times10^{6} \text{ V/sec}$$

$$S = 2\pi f V_m$$

i.e. $0.5\times10^{6} = 2\pi\times6.631\times10^{3}\times V_m$

$\therefore$ $V_m = \mathbf{12\ V}$

ii) $S = 0.5\times10^{6}$ V/sec., $V_m = 7$ V

$$S = 2\pi f_m V_m \text{ i.e. } f_m = \frac{0.5\times10^{6}}{2\pi\times7}$$

$\therefore$ $f_m = \mathbf{11.368\ kHz}$

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Problem on Opamp Bias Current:

For a particular op-amp, the input offset current is 20 nA while input bias current is 60 nA. Calculate the values of two input bias currents.

Sol. : $I_{ios} = 20$ nA, $I_b = 60$ nA

Now $I_{ios} = I_{b1} - I_{b2} = 20$

and $I_b = \frac{I_{b1} + I_{b2}}{2} = 60$

$\therefore \quad I_{b1} + I_{b2} = 120 \quad$ i.e. $\quad 2I_{b1} = 140$

i.e. $I_{b1} = \mathbf{70\ nA}$

$I_{b2} = \mathbf{50\ nA}$

Problem on Opamp Saturation Property:

A sine wave of 0.5 V peak voltage is applied to an inverting amplifier using $R_1 = 10$ kΩ and $R_f = 50$ kΩ. It uses the supply voltages of ± 12 V. Determine the output and sketch the waveform.
If now the amplitude of input sine wave is increased to 5 V, what will be the output ? Is it practically possible ? Sketch the waveform.

Sol. : Case 1 : For an inverting amplifier.

$$\text{Gain} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} = \frac{-50}{10} = -5$$

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Now V_m = 0.5 V for the input hence

$$(V_o)_m = (V_{in})_m \times \text{Gain}$$

$$= 0.5 \times 5 = \mathbf{2.5\ V\ peak}$$

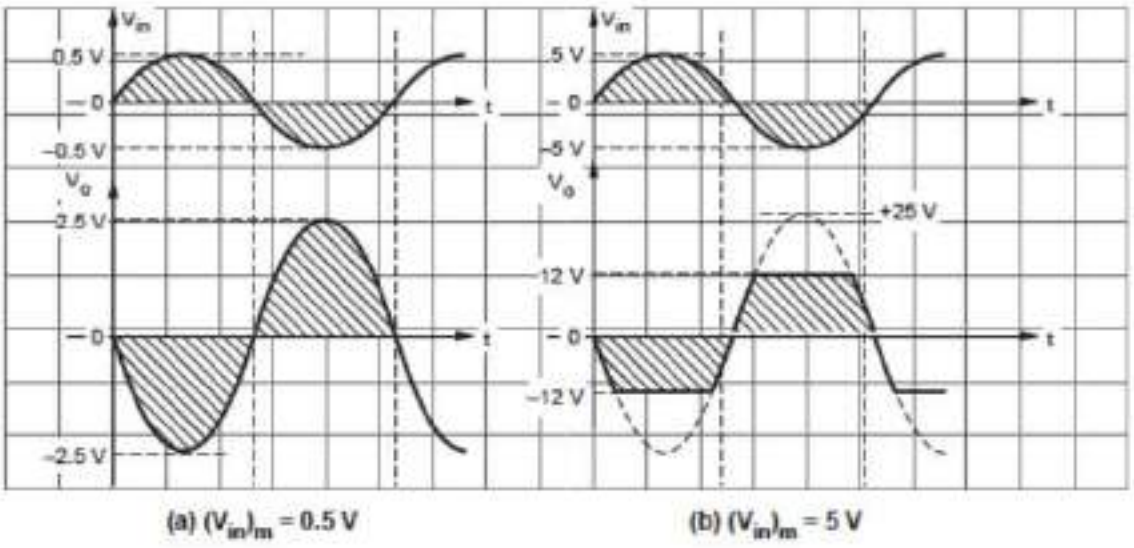
The input and output waveforms are inverted with respect to each other and are shown in the Fig. (a).

Case 2 : Now V_m = 5 V for the input hence,

$$(V_o)_m = (V_{in})_m \times \text{Gain} = 5 \times 5 = 25 \text{ V peak}$$

But op-amp output saturates at ± 12 V i.e. at supply voltages used. So portion above ± 12 V and below – 12 V will be clipped off from the output. So 25 V peak output is not practically possible. The input and output waveforms are shown in the Fig. (b).

In both cases, there exists a phase shift of 180° between input and output.



(a) $(V_{in})_m$ = 0.5 V (b) $(V_{in})_m$ = 5 V

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Problem on Opamp Inverting Amplifier:

An op-amp is used as an inverting amplifier to amplify an input sine wave of amplitude 100 mV (peak to peak). The input resistance R_1 = 1 kΩ and feedback resistance R_f =10 kΩ. Calculate the voltage gain and sketch the output waveform to scale.

VTU : March-05, Marks 6

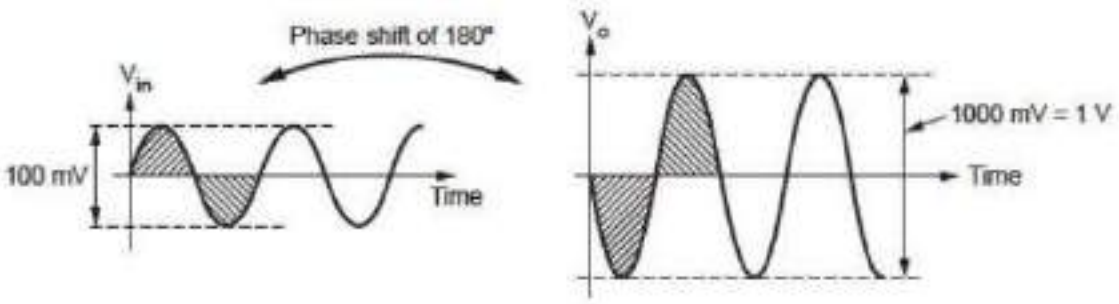
Sol. : Given, $R_1 = 1\ k\Omega$, $R_f = 10\ k\Omega$, $V_{in} = 100 \times 10^{-3}$ V

Voltage gain $A_f = \dfrac{V_o}{V_{in}} = \dfrac{-R_f}{R_1}$ i.e. $V_o = \dfrac{-R_f}{R_1} \times V_{in}$

$$\therefore \quad V_o = \frac{-10\times10^3}{1\times10^3}\times100\times10^{-3} = \mathbf{-1\ V}$$

Voltage gain $A_f = \dfrac{-R_f}{R_1} = -\dfrac{10\times10^3}{1\times10^3} = \mathbf{-10}$

The waveforms are shown in the Fig.



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Problem on Opamp Inverting Amplifier:

An inverting amplifier circuit has input series resistor of 20 kΩ, feedback resistor of 100 kΩ and a load resistor of 50 kΩ. Draw the circuit and calculate the input current, load current, and the output voltage when the applied input voltage is equal to + 1.5 V.

VTU : Aug.-07, Marks 8

Sol. : $R_1 = 20\ k\Omega$, $R_f = 100\ k\Omega$, $R_L = 50\ k\Omega$, $V_{in} = 1.5\ V$

The circuit is shown in the Fig. 3.14.4.

The node A is grounded hence node B is at virtual ground.

$$\therefore \quad V_A = V_B = 0\ V$$

$$\therefore \quad I_1 = \frac{V_{in} - V_B}{R_1}$$

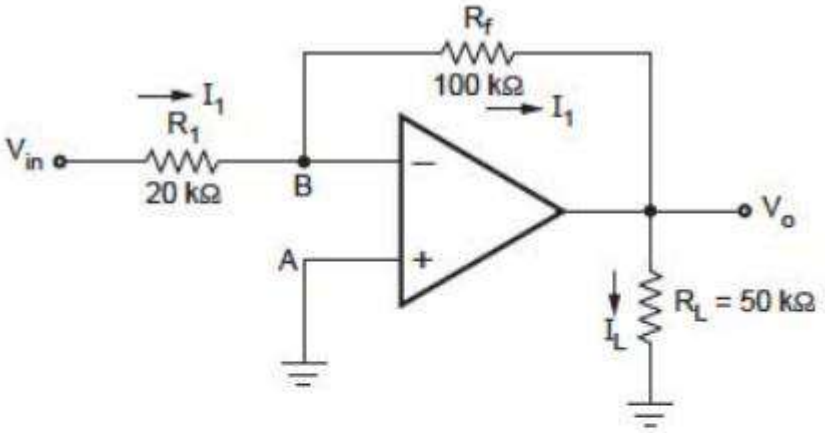

Fig. 3.14.4

$$= \frac{1.5 - 0}{20 \times 10^3} = 75\ \mu A \quad \text{... Input current}$$

The op-amp input current is zero hence same current I_1 passes through the resistance R_f.

$$\therefore \quad I_1 = \frac{V_B - V_o}{R_f}$$

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i.e. $75\times10^{-6} = \dfrac{0-V_o}{100\times10^3}$

$\therefore \quad V_o = -75\times10^{-6}\times100\times10^3$

$= -7.5\ V$ ... Output voltage

$\therefore \quad I_L = \dfrac{V_o}{R_L} = \dfrac{-7.5}{50\times10^3}$

$= -0.15\ mA$ ... Load current

The negative sign indicates that I_L flows from ground to output terminal i.e. upwards as V_o is negative.

Problem on Opamp Non Inverting Amplifier:

Find the gain and output voltage for a non-inverting amplifier using op-amp when input voltage is i) + 0.5 V ii) – 3 V. Assume supply voltage employed is ± 12 V, R_f = 10 kΩ, R_1 = 1 kΩ. **VTU : Jan.-16, Marks 4**

Sol. : The gain is,

$$\text{Gain} = 1 + \frac{R_f}{R_1} = 1 + \frac{10}{1} = \mathbf{11}$$

For $V_{in} = 0.5\ V$, $V_o = 11\times0.5 = \mathbf{5.5\ V}$

For $V_{in} = -3\ V$, $V_o = -3\times11 = \mathbf{-33\ V}$

But – 33 V is not possible. Output will saturate at – 12 V and remaining portion will be clipped off from the output.

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Problem on Opamp Inverting and Non Inverting Amplifier:

Design an inverting and non inverting operational amplifier to have a gain of 15.

VTU : Jan.-18, Marks 5

Sol. : Inverting amplifier : It is shown in the Fig. (a).

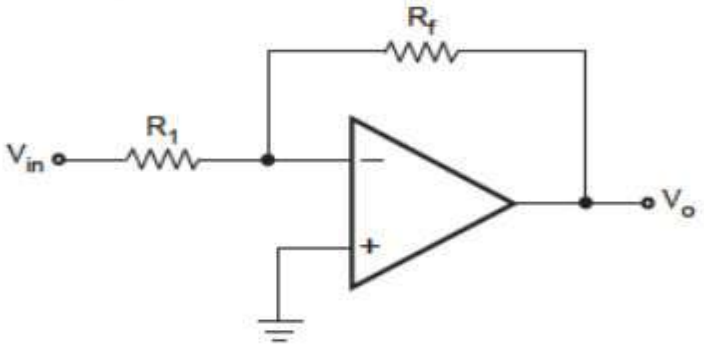

Fig. (a)

$$\text{Gain} = \left|-\frac{R_f}{R_1}\right| = 15$$

$\therefore \quad R_f = 15\, R_1$

Choose $R_1 = 10\ k\Omega$

$\therefore \quad R_f = 150\ k\Omega$

Noninverting amplifier : It is shown in the Fig. (b).

$$\text{Gain} = 1+\frac{R_f}{R_1} = 15$$

$$\therefore \quad \frac{R_f}{R_1} = 14$$

Choose $R_1 = 10\ k\Omega$

$\therefore \quad R_f = 140\ k\Omega$

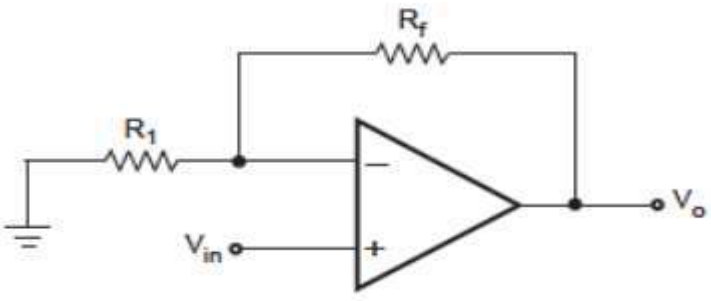

Fig. (b)

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Problem on Opamp Voltage Follower:

The input to the op-amp shown in Fig. at the non inverting terminal is 10 sin 10t Volts. Draw the output waveform indicating time period and maximum value. **VTU : June-12, Marks 4**

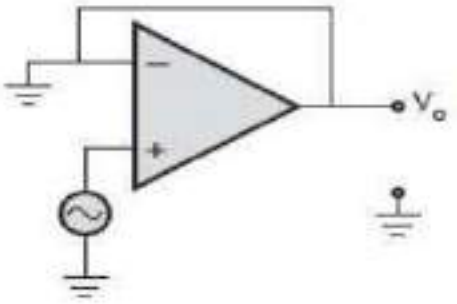

Fig.

Sol. : The circuit is voltage follower hence $V_o = V_{in}$.

$$\therefore \quad V_o = 10 \sin 10\,t$$

Maximum value = **10 V**

$$\omega = 10 = \frac{2\pi}{T}$$

$$\therefore \quad T = \mathbf{0.6283}\ \text{sec.}$$

The waveform is shown in the Fig. (a)

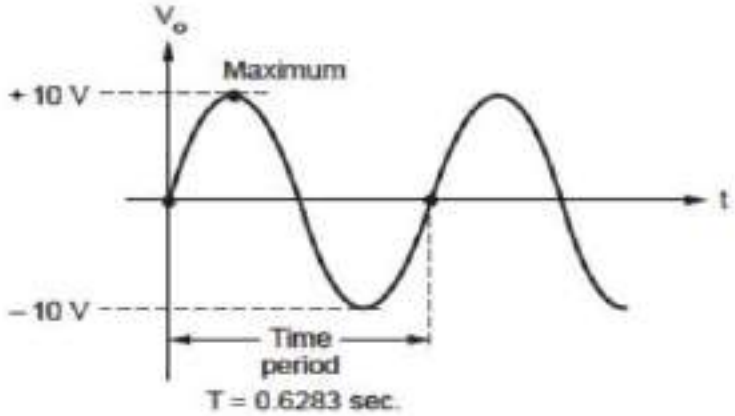

Fig. (a)

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Problem on Opamp Inverting Summer:

Calculate the output voltage of a three input inverting summing amplifier, given $R_1 = 200\ k\Omega$, $R_2 = 250\ k\Omega$, $R_3 = 500\ k\Omega$, $R_f = 1\ M\Omega$, $V_1 = -2\ V$, $V_2 = -1\ V$ *and* $V_3 = +3\ V$. **VTU : July-02, 03, 04, 08, 16, Marks 4**

Sol. : The circuit is shown in the Fig.

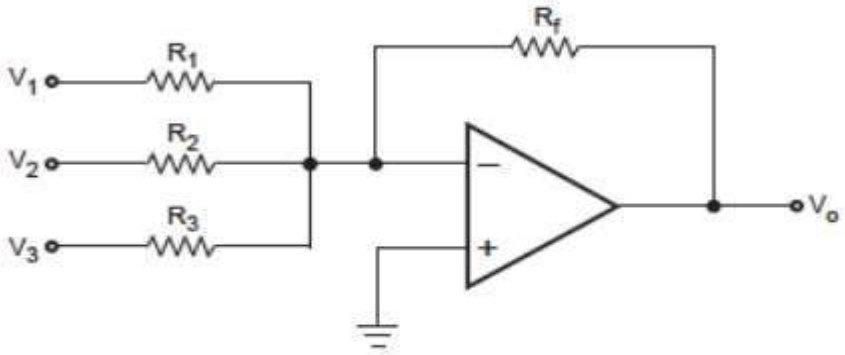


Fig.

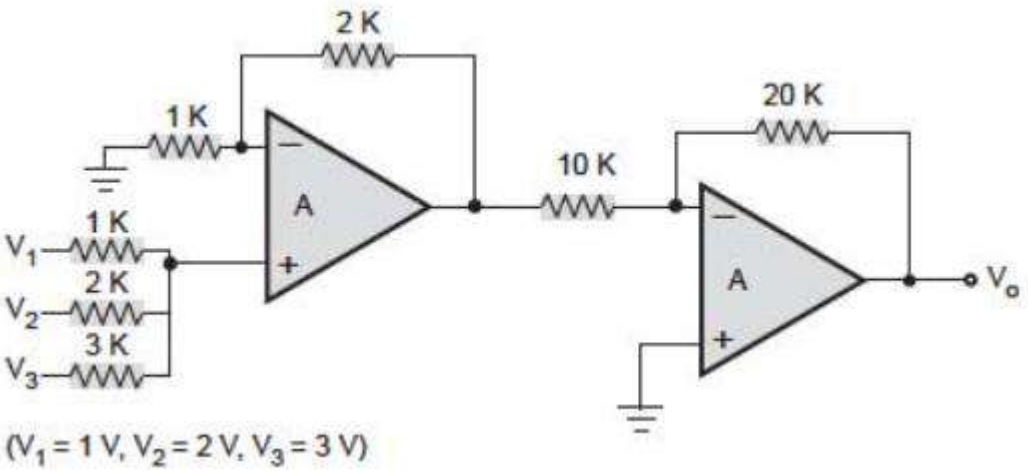
The output is given by,

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

$$= -\left[\frac{1\times10^6}{200\times10^3}(-2) + \frac{1\times10^6}{250\times10^3}(-1) + \frac{1\times10^6}{500\times10^3}(+3)\right]$$

$$= -[-10-4+6] = -[-8] = +\mathbf{8\ V}$$

Calculate the output voltage of the circuit given in Fig. **VTU : Feb.-09, Marks 8**



$(V_1 = 1\ V, V_2 = 2\ V, V_3 = 3\ V)$

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Sol. : Use Superposition theorem and consider each input acting separately.

Case 1 : V_1 acting, V_2 and V_3 grounded.

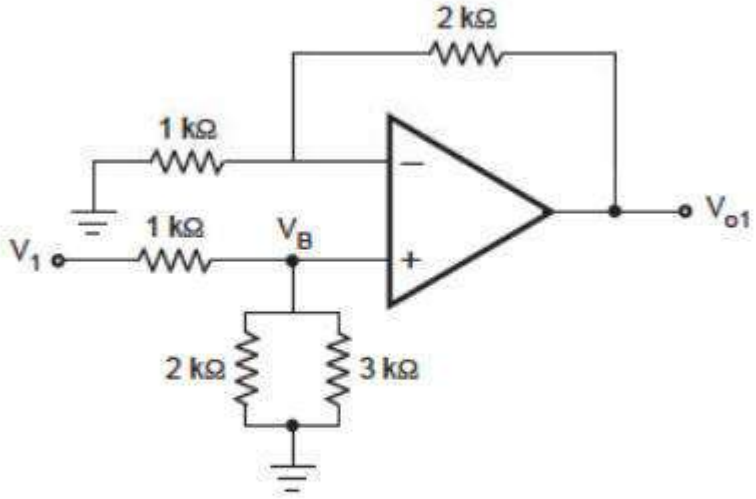

Fig. (a)

This is noninverting amplifier with $R_f = 2$ kΩ, $R_1 = 1\Omega$

$$\therefore \quad V_{o1} = \left[1 + \frac{R_f}{R_1}\right] V_B$$

$$V_B = \frac{V_1 [2\ k\Omega \parallel 3k\Omega]}{1\,k\Omega + [2\ k\Omega \parallel 3k\Omega]}$$

$$= 0.5454\ V_1$$

$$\therefore \quad V_{o1} = \left[1 + \frac{2}{1}\right] \times 0.5454\, V_1 = \mathbf{1.6363\ V_1}$$

Case 2 : V_2 acting, V_1 and V_3 grounded.

$1\,k\Omega \mid 3\,k\Omega = 750\ \Omega$

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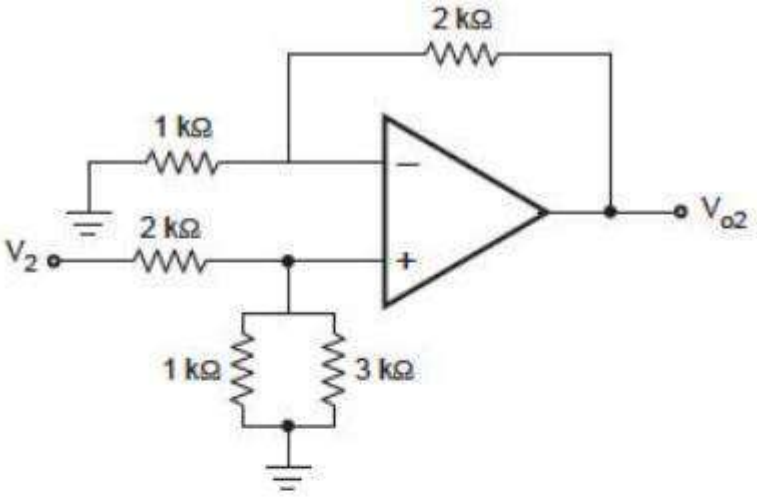

Fig. 3.17.5 (b)

$$\therefore \quad V_B = \frac{V_2 \times 750}{\left[2\times10^3 + 750\right]} = 0.2727\ V_2$$

$$\therefore \quad V_{o2} = \left[1 + \frac{R_f}{R_1}\right] V_B$$

$$= \left[1 + \frac{2\times10^3}{1\times10^3}\right] 0.2727\, V_2$$

$$= \mathbf{0.8181\ V_2}$$

Case 3 : V_3 acting, V_1 and V_2 grounded.

$1\text{k}\Omega \| 2\ \text{k}\Omega = 666.667\,\Omega$

$$\therefore \quad V_B = \frac{V_3 \times 666.667}{\left[3\times10^3 + 666.667\right]}$$

$$= 0.1818\ V_3$$

$$\therefore \quad V_{o3} = \left[1 + \frac{R_f}{R_1}\right] V_B$$

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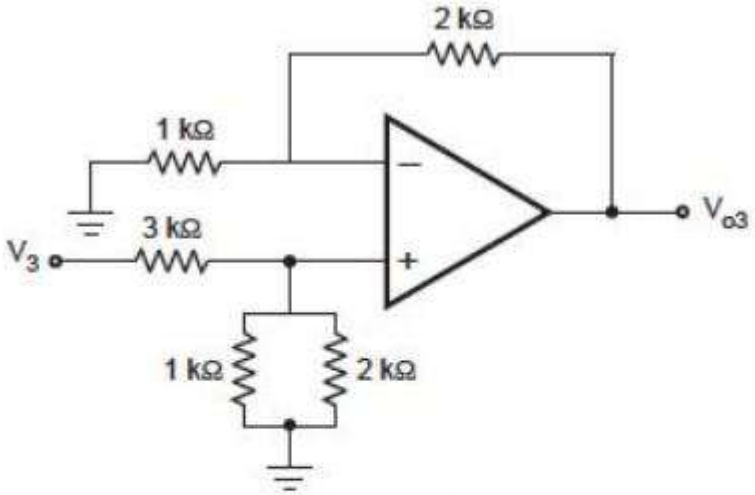

Fig. (c)

$$= \left[1 + \frac{2\times10^3}{1\times10^3}\right] \times 0.1818\, V_3 = 0.5454\, V_3$$

Now the voltage $(V_{o1} + V_{o2} + V_{o3})$ is applied to inverting amplifier as shown in the Fig. (d)

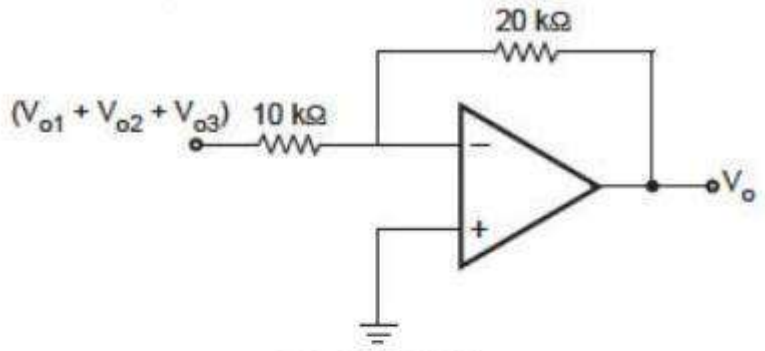

Fig. 3.17.5 (d)

$$\therefore \quad V_o = -\frac{R_f}{R_1}(V_{o1} + V_{o2} + V_{o3})$$

$$\therefore \quad V_o = \frac{-20}{10}[1.6363\, V_1 + 0.8181\, V_2 + 0.5454\, V_3)$$

$$\therefore \quad V_o = -3.2726\, V_1 - 1.6362\, V_2 - 1.0909\, V_3$$

with $V_1 = 1$ V, $V_2 = 2$ V and $V_3 = 3$ V

$$\therefore \quad V_o = -3.2726 - [1.6362 \times 2] - [1.0909 \times 3]$$

$$= \mathbf{-9.8178\ V}$$

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Problem on Opamp Inverting Summer:

Find the output voltage for the circuit below.

VTU : Aug.-09, Marks 6

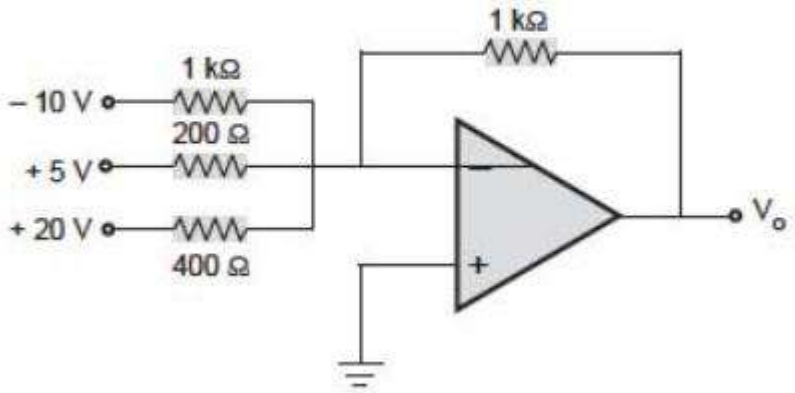

Fig.

Sol. : The circuit is inverting summing amplifier with,

$$R_1 = 1\ k\Omega,\quad R_2 = 200\ \Omega,\ R_3 = 400\ \Omega,\quad R_f = 1\ k\Omega$$

$$V_1 = -10\ V,\qquad V_2 = 5\ V,\qquad V_3 = 20\ V$$

$$\therefore \quad V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

$$= -\left[\frac{1000}{1\times10^3} \times (-10) + \frac{1000}{200} \times 5 + \frac{1000}{400} \times 20\right]$$

$$= -\ \mathbf{65\ V}$$

But op-amp can not produce output greater than the saturation voltages according to its saturation property.

$$\therefore \quad V_o = \pm V_{sat}$$

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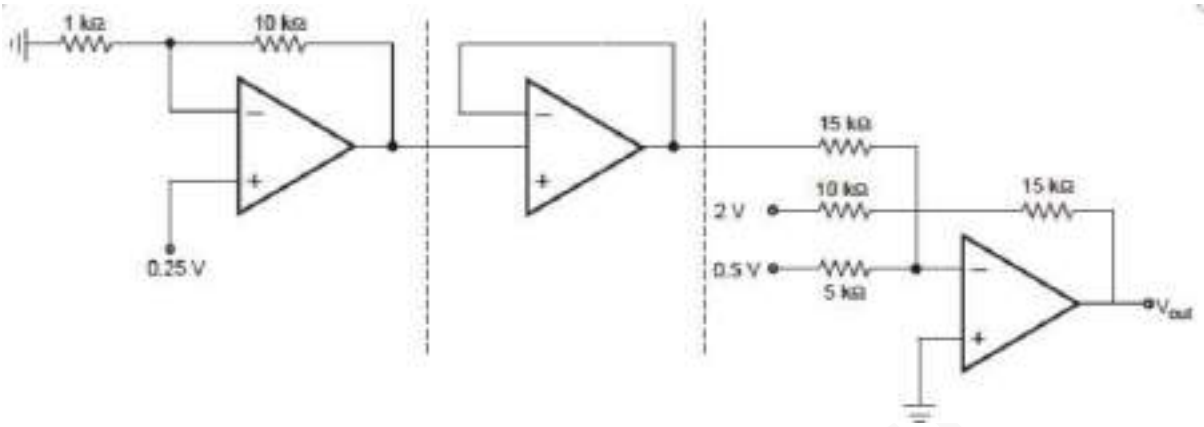
Find the output of the following op-amp circuit. **VTU : Jan.-17, Marks 5**



Sol. : First op-amp circuit is noninverting amplifier.

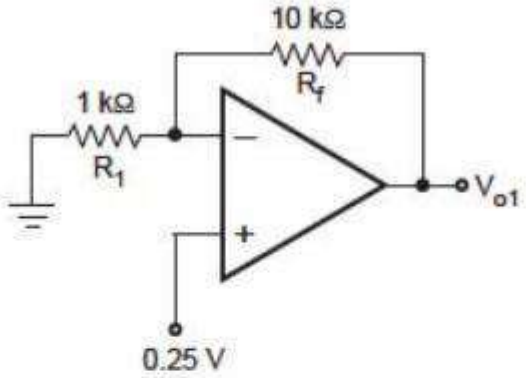


Fig.

$$V_{o1} = 0.25\left(1+\frac{R_f}{R_1}\right)$$

$$= 0.25\left(1+\frac{10}{1}\right) = 2.75 \text{ V}$$

The second op-amp circuit is voltage follower.

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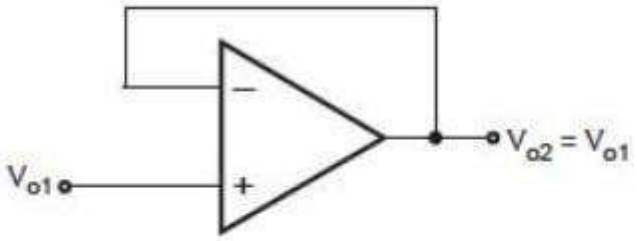

Fig.

$\therefore \quad V_{o2} = V_{o1} = 2.75\ V$

The third op-amp circuit is inverting summing amplifier.

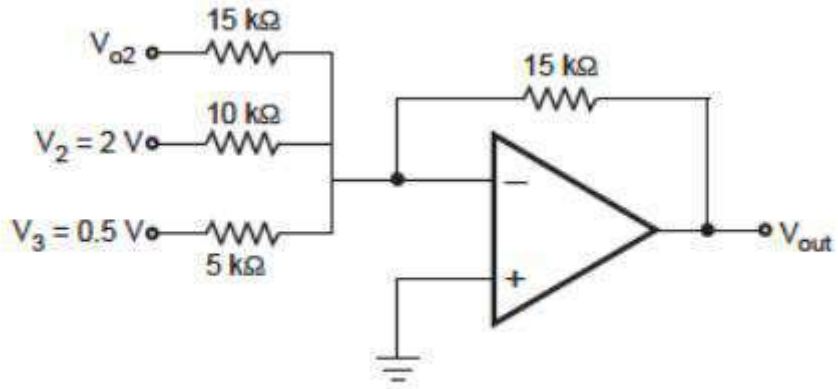

Fig.

$$\therefore \quad V_{out} = -\left[\frac{R_f}{R_1}V_{o2} + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

$$= \left[\frac{15}{15}\times 2.75 + \frac{15}{10}\times 2 + \frac{15}{5}\times 0.5\right]$$

$$= -7.25\ V$$

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Design an adder circuit using op-amp to obtain an output voltage of $V_0 = 2[0.1\,V_1 + 0.5\,V_2 + 2\,V_3]$, where V_1, V_2 and V_3 are input voltages. Draw the circuit diagram. **VTU : July 15, Marks 8**

Sol. : Given $V_o = 0.2\,V_1 + V_2 + 4\,V_3$

Let us design inverting summer with $V_o = -\,[0.2\,V_1 + V_2 + 4\,V_3]$ and then use inverting amplifier with unity gain.

For $$V_o = -\,[0.2\,V_1 + V_2 + 4V_3]$$

$$= -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

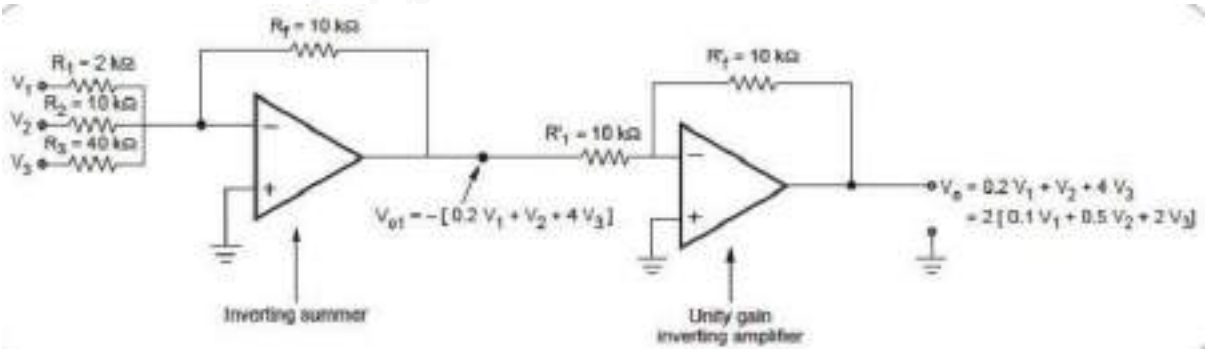
$\therefore$ $$\frac{R_f}{R_1} = 0.2, \quad \frac{R_f}{R_2} = 1, \quad \frac{R_f}{R_3} = 4,$$

select $R_f = 10\ k\Omega$

$\therefore R_1 = 2\ k\Omega, \quad R_2 = 10\ k\Omega, \quad R_3 = 40\ k\Omega$

Then use inverting amplifier with $R'_f = R'_1 = 10\ k\Omega$ so its gain is $-R'_f / R'_1 = -1$.

The designed circuit is shown in the Fig.



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Problem on Opamp Subtractor:

Design the op-amp circuit which can give the output as

$V_o = 2V_1 - 3V_2 + 4V_3 - 5V_4$

Sol. : The positive and negative terms can be added separately using two adders and then subtractor can be used.

For $2V_1 + 4V_3$, let $R_{f1} = 100\ k\Omega$

$$V_{o1} = -\left(\frac{R_{f1}}{R_1}V_1 + \frac{R_{f1}}{R_3}V_3\right)$$

$$\therefore \quad \frac{R_{f1}}{R_1} = 2 \quad \text{hence } R_1 = 50\ k\Omega$$

$$\text{and} \quad \frac{R_{f1}}{R_3} = 4 \text{ hence } R_3 = 25\ k\Omega$$

For $3V_2 + 5V_4$, let $R_{f2} = 120\ k\Omega$

$$V_{o2} = -\left(\frac{R_{f2}}{R_2}V_1 + \frac{R_{f2}}{R_4}V_3\right)$$

$$\therefore \quad \frac{R_{f2}}{R_2} = 3 \text{ hence } R_2 = 40\ k\Omega$$

$$\text{and} \quad \frac{R_{f2}}{R_4} = 5 \text{ hence } R_4 = 24\ k\Omega$$

Use the subtractor with all the resistances of same value of $R = 100\ k\Omega$.

Hence the output of the subtractor is $V_o = V_{o2} - V_{o1}$ where V_{o2} and V_{o1} are the two inputs of the subtractor, derived from the previous adders.

The output voltage is,

$$\begin{aligned} V_o &= V_{o2} - V_{o1} \\ &= -3V_2 - 5V_4 - (-2V_1 - 4V_3) \\ &= 2V_1 - 3V_2 + 4V_3 - 5V_4 \end{aligned}$$

This is the required output.

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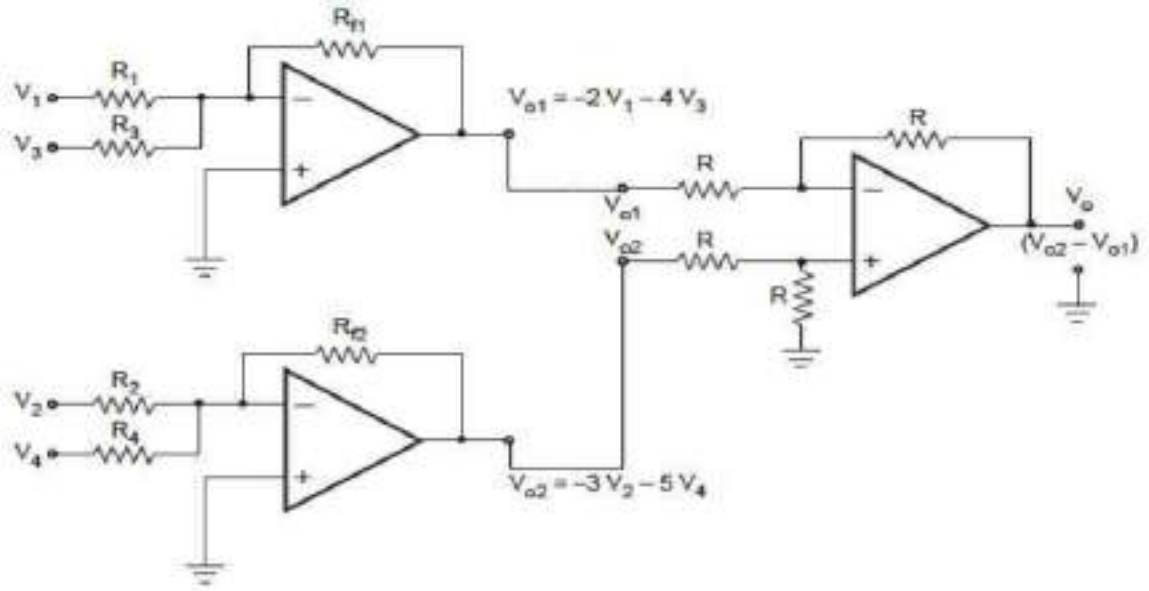

Problem on Opamp Integrator:

A sinusoidal signal with peak value 6 mV and 2 kHz frequency is applied to the input of an ideal op-amp integrator with $R_1 = 100\ k\Omega$ and $C_f = 1\ \mu F$. Find the output voltage. **VTU : Feb.-06, Marks 6**

Sol. : For an ideal integrator

$$V_o = -\frac{1}{R_1 C_f}\int_0^t V_{in}\, dt$$

Now $R_1 = 100\ k\Omega$, $C_f = 1\mu F$, $V_{in} = V_m \sin \omega t$

where $V_m = 6\ mV$

and $\omega = 2\pi f = 2\pi \times 2 \times 10^3 = 4\pi \times 10^3\ rad/s$

$$\therefore V_o = -\frac{1}{100 \times 10^3 \times 1 \times 10^{-6}}\int_0^t 6 \times 10^{-3} \sin\left(4\pi \times 10^3 t\right) dt$$

$$= -0.06\left[\frac{-\cos\left(4\pi \times 10^3\, t\right)}{4\pi \times 10^3}\right]_0^t$$

$$= \mathbf{4.77 \times 10^{-6}\left[\cos(4000\pi t) - 1\right] V}$$

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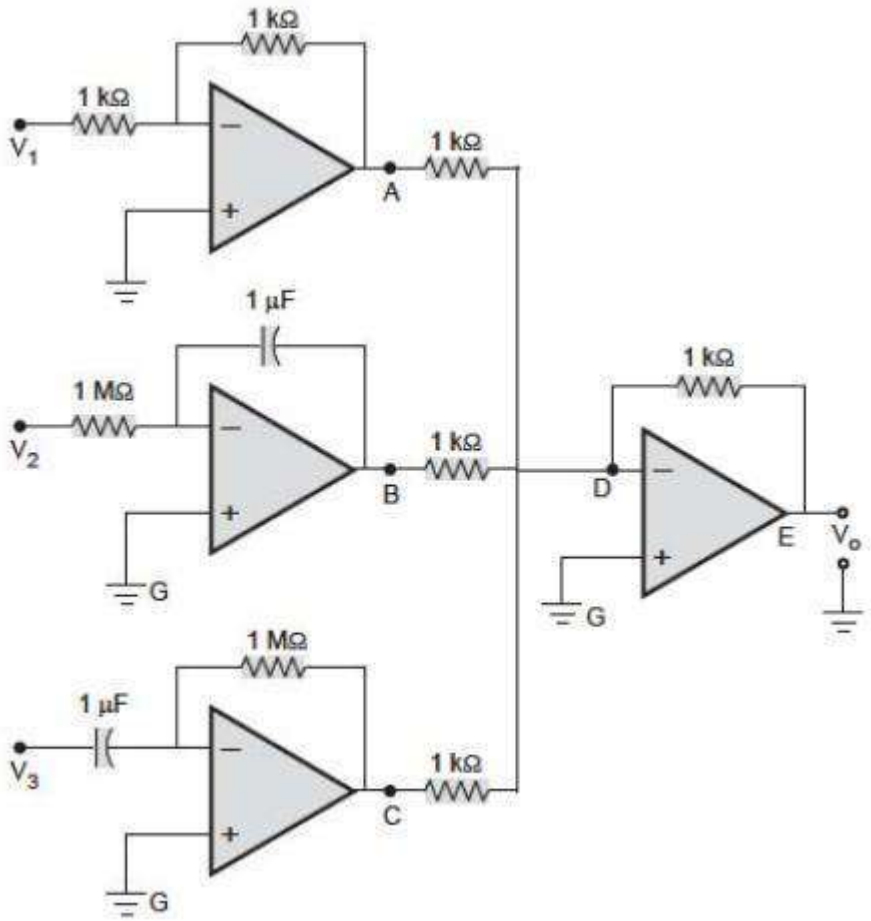
Write expression for output voltage at points A, B, C, D and E as shown in Fig.

VTU : Jan.-15, Marks 10



Sol. : Op-amp 1 is inverting amplifier hence

$$V_A = \frac{-R_f}{R_1} V_1$$

$$\therefore \quad V_A = \frac{-1\times10^3}{1\times10^3} V_1 = -V_1$$

Op-amp 2 is an integrator

hence $$V_B = -\frac{1}{R_f C_f} \int V_2 \, dt$$

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$$\therefore \quad V_B = -\frac{1}{1\times10^6\times1\times10^{-6}}\int V_2\ dt$$

$$= -\int V_2\ dt$$

Op-amp 3 is a differentiator

hence $$V_C = -R_1 C_f \frac{dV_3}{dt}$$

$$\therefore \quad V_C = -1\times10^6\times1\times10^{-6}\frac{dV_3}{dt} = \frac{-dV_3}{dt}$$

Op-amp 4 is inverting summing amplifier hence,

$$V_E = -\left[\frac{R_f}{R_1}V_A + \frac{R_f}{R_2}V_B + \frac{R_f}{R_3}V_C\right]$$

$$\ldots R_1 = R_2 = R_3 = 1\ k\Omega$$

$$= -\frac{1\times10^3}{1\times10^3}[V_A + V_B + V_C]$$

$$= V_1 + \int V_2\ dt + \frac{dV_3}{dt}$$

The point D is at virtual ground hence $V_D = 0$ V.

Question Bank *Dr.Dankan Gowda V M.Tech.,Ph.D*
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MODULE-4

BJT Applications, Feedback Amplifiers and Oscillators

BJT as an amplifier, BJT as a switch, Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay (4.4 and 4.5 of Text 2)

Feedback Amplifiers- Principle, Properties and advantages of Negative Feedback, Types of feedback, voltage series feedback, Gain stability with feedback (7.1-7.3 of Text 1)

Oscillators- Barkhaunsen's criteria for oscillation, RC phase shift oscillator, Wien Bridge oscillator (7.7-7.9 of Text 1)

IC 555 Timer and Astable Oscillator using IC 555 (17.2 and 17.3 of Text 1)

1. Text 1 : D.P Kothari, LJ Nagarath, "Basic Electronics", 2nd edition, Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

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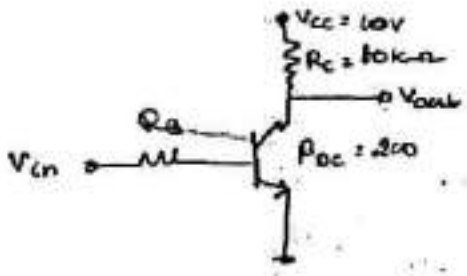
Topic 1. BJT

1. With neat circuit diagram explain how transistor is used as an voltage amplifier. Derive an equation for Av. **(08 Marks) Dec 2018-Jan 2019./ (08 Marks) Dec 2019-Jan 2020.**

2. With neat circuit diagram explain how transistor can be used to switch an LED ON/OFF and give the necessary equation. **(8 Marks) Dec 2018-Jan 2019.**

3. The transistor in common emitter configuration is shown in Fig. With R_c=10KΩ and β_{dc}=200. Determine
   i. V_{CE} at V_{in}=0
   ii. $I_{B(min)}$ to Saturate the collector current
   iii. $R_{B(max)}$ when V_{in}=5V.

   $V_{CE(sat)}$ can be neglected. **(4 Marks) Dec 2018-Jan 2019.**



4. What is an amplifier? Explain how transistor can be used as an amplifier. **(6 Marks) June-July 2019./ (08 Marks) MQP-2**
5. The transistor in common emitter (CE) configuration is shown in Fig. With R_c=1KΩ and β_{dc}=125. Determine

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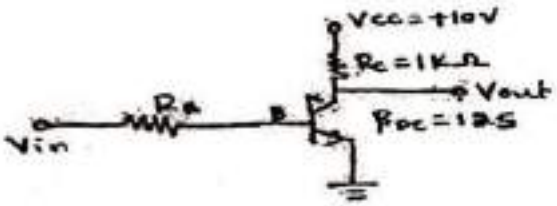
i. V_{CE} at V_{in}=0
ii. $I_{B(min)}$ to Saturate the collector current
iii. $R_{B(max)}$ when V_{in}=8 V.

$V_{CE(sat)}$ can be neglected. **(4 Marks) Dec 2019-Jan 2020.**



6. Explain the operation of BJT as an amplifier and as a switch. **(08 Marks) MQP-1/(10 Marks) MQP-3**

7. Briefly explain how a transistor is used as an electronic switch. **(06 Marks) MQP-2**

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Topic 2. Feedback Amplifiers

1. Explain the voltage series feedback circuit and derive an equation for voltage gain Av with feedback. **(4 Marks) Dec 2018-Jan 2019./ (6 Marks) June-July 2019./ (04 Marks) Dec 2019-Jan 2020./ (06 Marks) MQP-1**

2. What is feedback amplifier? what are the properties of negative feedback amplifier ? **(6 Marks) June-July 2019.**

3. What is a feedback amplifier ? with a necessary diagrams and equation, Briefly explain different types of feedback amplifiers. **(06 Marks) MQP-1/(12 Marks) MQP-2.**

4. An amplifier has a high frequency response described by $A = \frac{A_0}{1+(\frac{j\omega}{\omega_2})}$. Where in A_0=1000, ω_2=104 rad/sec. Find the feedback factor which will raise the upper corner frequency $\omega_2$to 105 Hz. What is the corresponding gain of the amplifier? Find also the gain bandwidth product in this case. **(04 Marks) MQP-3.**

5. List the advantages of negative feedback in an amplifier. Explain the voltage series feedback amplifier. Show that the gain bandwidth product for a feedback amplifier is constant. **(10 Marks) MQP-3.**

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Topic 3. Oscillators

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1. Explain RC phase-shift oscillator with circuit diagram and necessary equations. **(8 Marks) Dec 2018-Jan 2019/ (08 Marks) Dec 2019-Jan 2020./ (06 Marks) MQP-1/(06 Marks) MQP-3.**

2. Design a RC Phase shift oscillator for a frequency of 1KHz. Draw the circuit diagram with designed values. **(6 Marks) June-July 2019.**

3. With a neat circuit diagram, explain the working of wein Bridge oscillator. **(6 Marks) June-July 2019./ (08 Marks) Dec 201-Jan 2020.**

4. Define an oscillator ? derive the equation for Wien bridge oscillator. **(08 Marks) MQP-2**

5. Explain the Barkhausen's criteria for oscillations. **(06 Marks) MQP-1**

6. The frequency sensitivity arms of the wein bridge oscillator uses C1=C2=0.01μF and R1=10KΩ while R2 is kept variable. The frequency is to be varied from 10K Hz to 50K Hz by varying R2. Find the minimum and maximum values of R2. **(04 Marks) MQP-3.**

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Topic 4. 555 Timer

1. Explain the operation of IC-555 as an Astable oscillator (astable operation) with neat circuit diagram and necessary equation. **(08 Marks) Dec 2018-Jan 2019./ (08 Marks) Dec 2019-Jan 2020./ (08 Marks) MQP-1/ (06 Marks) MQP-3.**

2. With a neat circuit diagram and waveforms, explain the working of 555 timers as an oscillator. **(8 Marks) June-July 2019.**

3. Explain how 555 timer can be used as an oscillator. **(06 Marks) MQP-2**

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MODULE-4
Topic 1. BJT

With neat circuit diagram explain how transistor is used as an voltage amplifier. Derive an equation for Av. (08 Marks) Dec 2018-Jan 2019./ (08 Marks) Dec 2019-Jan 2020.

What is an amplifier? Explain how transistor can be used as an amplifier. (6 Marks) June-July 2019./ (08 Marks) MQP-2

Refer next Question.

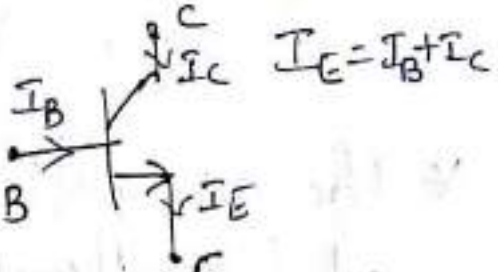
Explain the operation of BJT as an amplifier and as a switch. (08 Marks) MQP-1/(10 Marks) MQP-3

Soln:-

Amplifier:- Amplification is the process of Linearly increasing the amplitude of an Electrical Signal and is one of the major properties of transistor.

* Transistor amplifies Current because the collector current is equal to the base current multiplied by the Current gain (β).

i.e $\boxed{I_C = \beta I_B}$



* I_B is very Small Compared to I_C & I_E. i.e.

$\boxed{I_E \simeq I_C}$ Generally $I_B \rightarrow \mu A$
$I_C, I_E \rightarrow mA$

Voltage Amplification:-

Fig a. shows basic transistor amplifier Circuit with ac Source voltage V_s is Superimposed on the dc bias voltage V_{BB} by Capacitive Coupling.

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* The dc bias voltage V_{CC} is connected to the collector through the collector resistor (R_C).

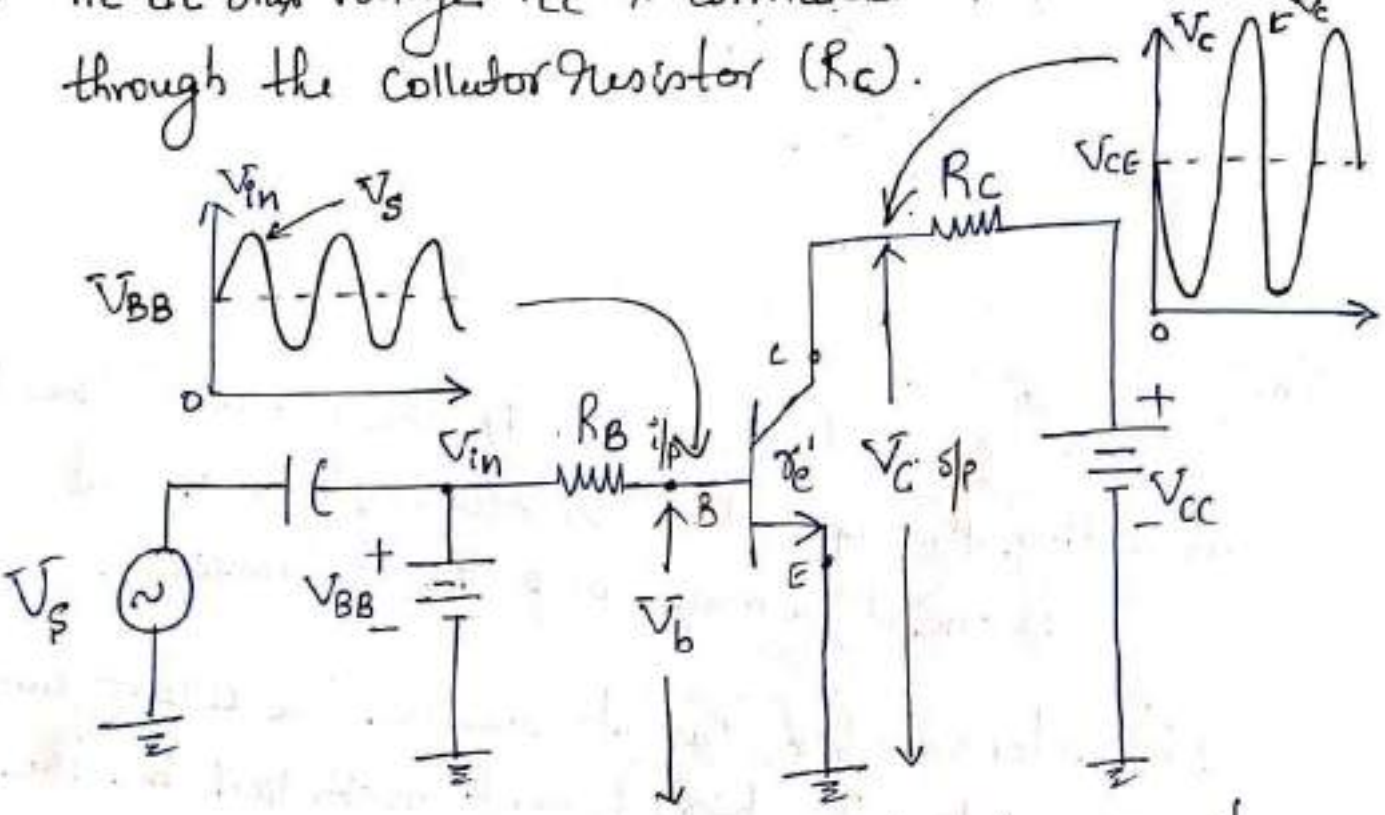
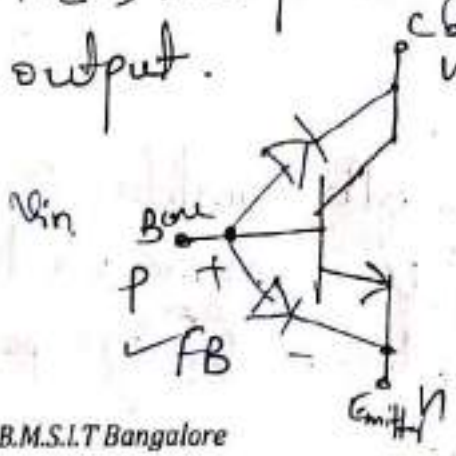


fig a:- BJT as Voltage Amplifier Circuit.

* The ac input voltage produces an ac base current which results in a much large ac collector current.
* The ac collector current (I_C) produces an ac voltage across R_C, thus producing an Amplified, but inverted output.
*



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* The Forward biased-base Emitter junction presents a very low resistance to the ac signal. and this internal ac Emitter resistance is designated by r_e'.

* The ac base voltage $V_b = I_e r_e'$ ← (1)

* The ac collector voltage V_c is equal to the ac voltage drop across R_c.

i.e $V_c = I_c R_c$ ← (2)

Since $I_e \cong I_c$

$V_c = I_e R_c$ ← (2a)

V_b is the transistor input voltage given by

$V_b = V_s - I_b R_B$ ← (1a)

* Voltage Gain is defined as the ratio of the output voltage to the input voltage. i.e

$$A_v = \frac{V_c}{V_b}$$

$$A_v = \frac{V_c}{V_b} \cong \frac{I_e R_c}{I_e r_e'} = \frac{R_c}{r_e'}$$

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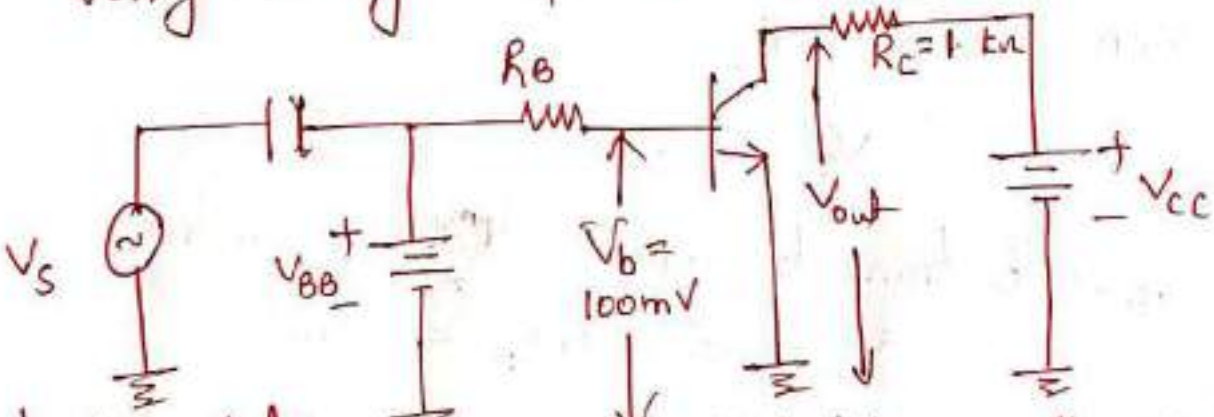
$$A_v \cong \frac{R_c}{r_e'}$$

Note: * Voltage gain depends on the values of R_c and r_e'.

* Choose R_c is always considerably large compared to r_e', the gain will be larger.

Problem. Determine the voltage gain and the ac output voltage in fig. if $r_e' = 50\Omega$.



and also what value of R_c will it take to have a voltage gain of 50.

Soln: The voltage gain is

$$A_v \cong \frac{R_c}{r_e'} = \frac{1\ k\Omega}{50} = \frac{1000}{50} = 20$$

$$\boxed{A_v = 20}$$

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∴ the ac output voltage is

$$V_{out} = A_v \cdot V_b = (20)(100m)$$

$$\boxed{V_{out} = 2 \text{ Volts (rms)}}$$

$R_C = ?$ to get $A_v = 50$

w.k.t $A_v = \frac{R_C}{r_e'}$

$$R_C = A_v \cdot r_e' = 50 \times 50$$

$$R_C = 2500\,\Omega$$

$$\therefore \boxed{R_C = 2.5\,k\Omega}$$

Use a Value of $R_C = 2.5k\Omega$ to get an Voltage gain $A_v = 20$.

Ans.

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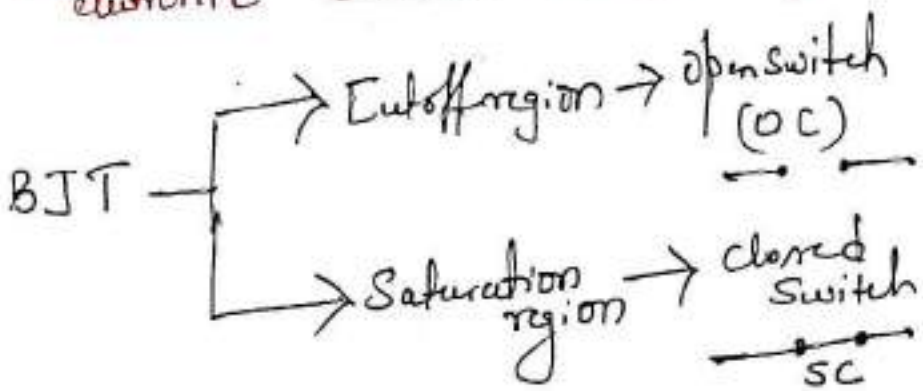
XP

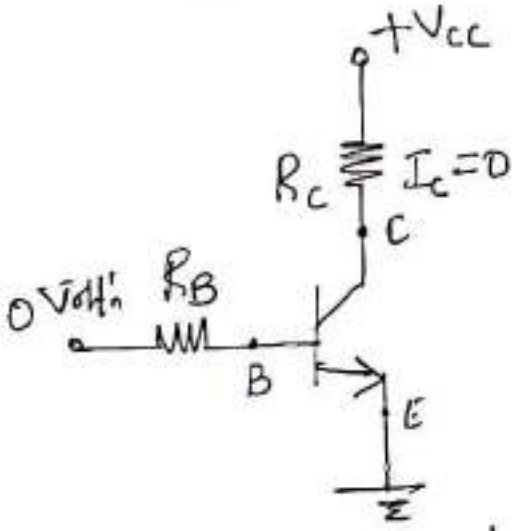
BJT as a Switch

Question. Briefly explain how a transistor is used as an electronic switch. (6M) MOP-2

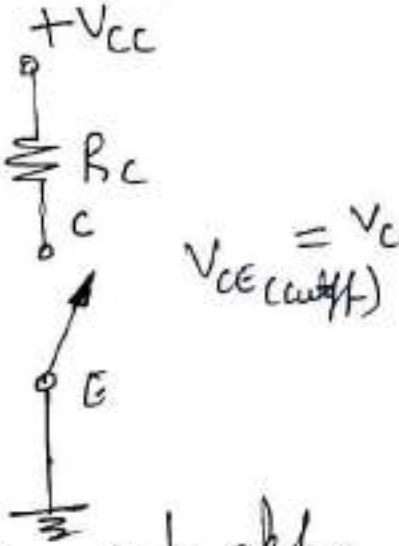
Soln:-



i. open Switch :-



(a) Cut-off - open Switch.



Equivalent ckt.

* In fig a. Transistor is in the cut-off region because the base-emitter junction is not forward biased.

i.e $I_B = 0A$ $\therefore I_C = \beta I_B = 0A$

$\therefore$ open ckt.

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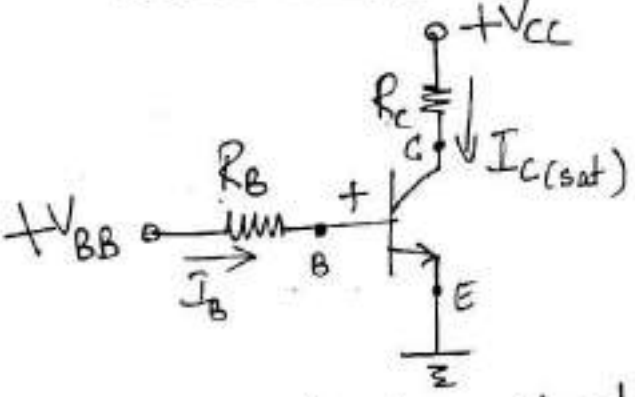
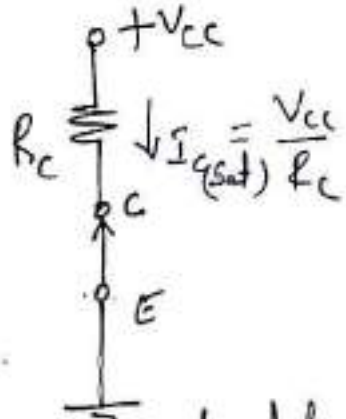
* This indicates an open ckt. Exist between Emitter and Collector terminal.

ii. Closed Switch :-



(b) Saturation - closed Switch.



Equivalent ckt.

* In fig b. the transistor in in Saturation region because the base-emitter junction and base collector junction are forward-biased and the base current (I_b) is made Large enough to cause the collector current to reach its Saturation value ($I_{C sat}$).

* This condition indicates an short Circuit between collector and Emitter.

* The small voltage drop b/w collector to Emitter terminal called $V_{CE(sat)}$)

generally $V_{CE(sat)} \simeq 0$ volts. (negligible)

A7

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Condition in Cutoff :-

a transistor is in cut-off region when the base emitter junction is not forward biased.

$$V_{CE(cutoff)} = V_{CC}$$

Condition in Saturation :- when the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is Saturated.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \simeq \frac{V_{CC}}{R_C}$$

$V_{CE(sat)}$ is very small compared to V_{CC} ∴ it can be neglected.

The Minimum value of Base current (I_B) needed to produce saturation is

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

I_B should be Significantly greaterthan $I_{B(min)}$ to Ensure that the transistor is Saturated.

A8.

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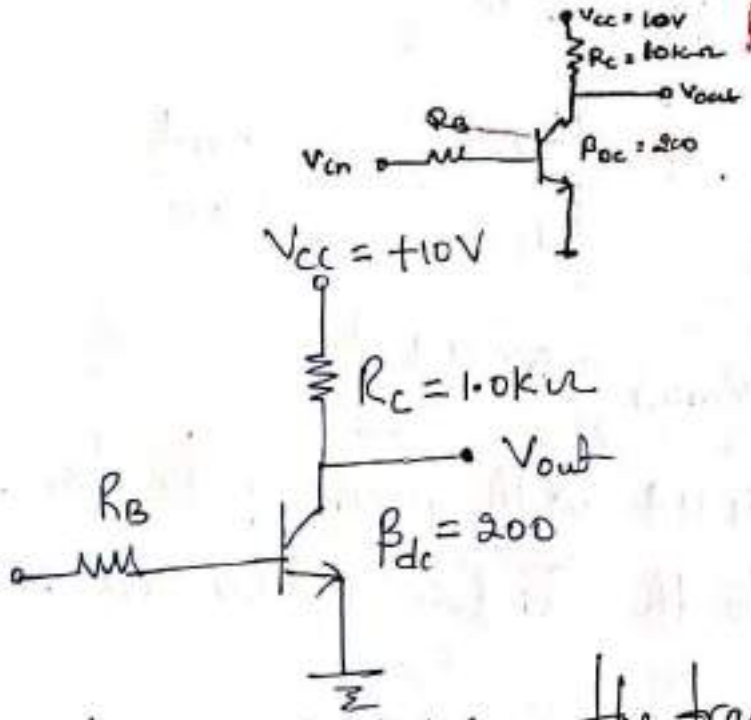
The transistor in common emitter configuration is shown in Fig. With R_c=10KΩ and β_{dc}=200. Determine

i. V_{CE} at V_{in}=0
ii. $I_{B(min)}$ to Saturate the collector current
iii. $R_{B(max)}$ when V_{in}=5V.

$V_{CE(sat)}$ can be neglected. **(4 Marks) Dec 2018-Jan 2019.**



Soln:-

$R_c = 1.0k\Omega$.

$V_{CC} = +10V$

$R_C = 1.0k\Omega$

V_{out}

R_B

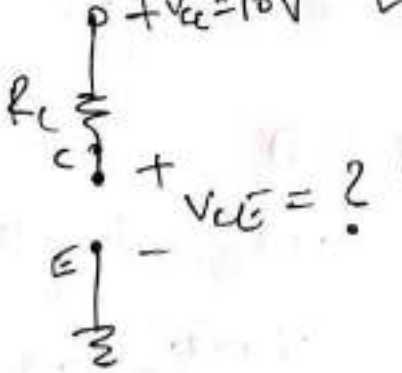
$\beta_{dc} = 200$

V_{IN}

E

Ex: When $V_{in} = 0$ volts, the transistor is in Cutoff region (acts like an open Switch)

and $\therefore$ $V_{CE(cutoff)} = V_{CC} = 10$ volts



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ii. Given $V_{CE(sat)} \rightarrow$ neglect $\simeq 0$ volts

$$\therefore I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10}{1.0k} = 10mA.$$

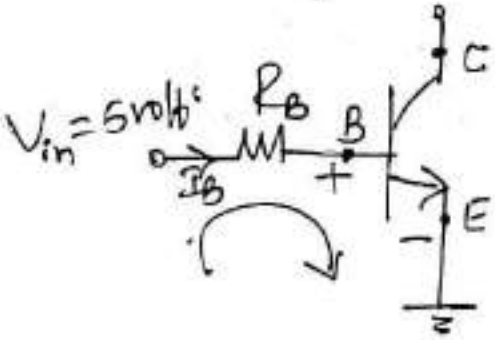
$$\boxed{I_{C(Sat)} = 10mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{10mA}{200}$$

$$\boxed{I_{B(min)} = 50\mu A}$$

$I_{B(min)} = 50\mu A$ is the necessary to drive the transistor to the point of saturation.

iii. $R_{B(max)} = ?$ $V_{in} = 5$ volts



When transistor is ON,
$V_{BE} \cong 0.7$ volts

KVL to i/p Loop.

$$V_{in} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B R_B = V_{in} - V_{BE} \Rightarrow R_B = \frac{V_{in} - V_{BE}}{I_B}$$

$$R_{B(max)} = \frac{V_{in} - V_{BE}}{I_{B(min)}} = \frac{5 - 0.7}{50\mu} = \frac{4.3}{50\mu}$$

$$\boxed{R_{B(max)} = 86k\Omega}$$

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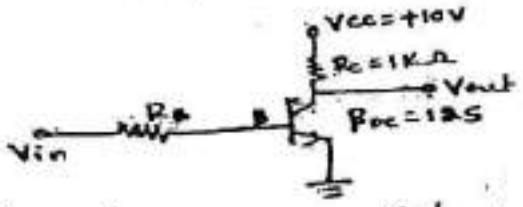
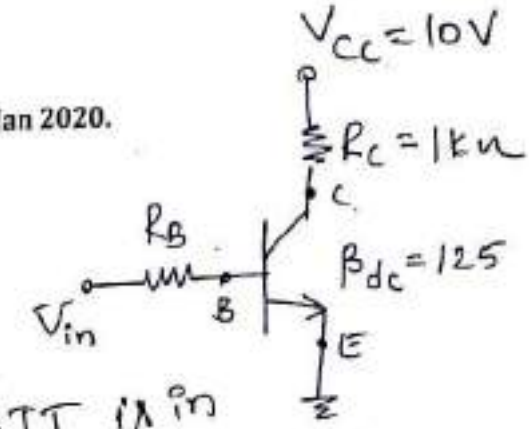
The transistor in common emitter (CE) configuration is shown in Fig. With R_c=1KΩ and β_{dc}=125. Determine

i. V_{CE} at V_{in}=0
ii. $I_{B(min)}$ to Saturate the collector current
iii. $R_{B(max)}$ when V_{in}=8 V,

$V_{CE(sat)}$ can be neglected. **(4 Marks) Dec 2019-Jan 2020.**





Soln:- i. when V_{in}=0 volts; BJT is in Cutoff region (acts as an open circuit).

$\therefore$ $\boxed{V_{CE} = V_{CC} = +10 \text{ volts}}$

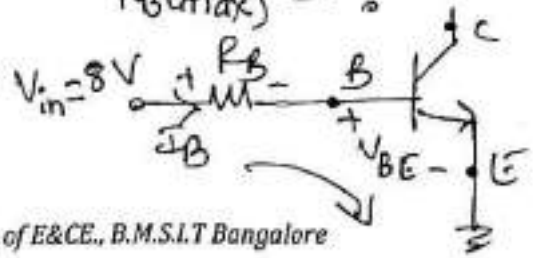
ii. $I_{B(min)} = \dfrac{I_{C(sat)}}{\beta_{dc}} = \dfrac{(V_{cc}/R_c)}{\beta_{dc}} = \dfrac{V_{cc}}{R_c \cdot \beta_{dc}}$

(given $V_{CE(sat)}$ is negligible)

$\therefore$ $I_{B(min)} = \dfrac{10}{(1K)(125)} = \dfrac{10}{1000 \times 125}$

$\boxed{I_{B(min)} = 80\mu A}$ required to saturate the collector current.

iii. $R_{B(max)}$ = ? when V_{in} = 8 volts



KCL input Loop

$V_{in} - I_B R_B - V_{BE} = 0$

V_{BE} = 0.7 volts (assume)

All

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$$I_B = \frac{V_{in} - V_{BE}}{R_B}$$

(or)

$$R_B = \frac{V_{in} - V_{BE}}{I_B}$$

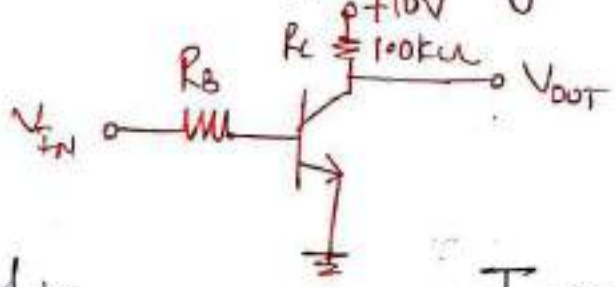
To get $R_{B(max)}$, I_B must be Minimum i.e $I_{B(min)}$

$$\therefore R_{B(max)} = \frac{V_{in} - V_{BE}}{I_{B(min)}} = \frac{8 - 0.7}{80\mu} = \frac{8 - 0.7}{80 \times 10^{-6}}$$

$$R_{B(max)} = 91.25 \times 10^3 \ \Omega$$

(or) $\boxed{R_{B(max)} = 91.25\ k\Omega}$

Question: Determine the Minimum value of I_B required to saturate the transistor in fig a. if $\beta_{dc} = 125$ and $V_{CE(sat)} = 0.2V$.



Soln:

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10 - 0.2}{1.0k} = \underline{\underline{9.8mA}}$$

$$I_{B(min)} = \frac{9.8 \times 10^{-3}}{125} = 78.4 \times 10^{-6}$$

$\boxed{I_{B(min)} = 78.4\mu A}$ required to saturate the transistor.

Application of a Transistor Switch

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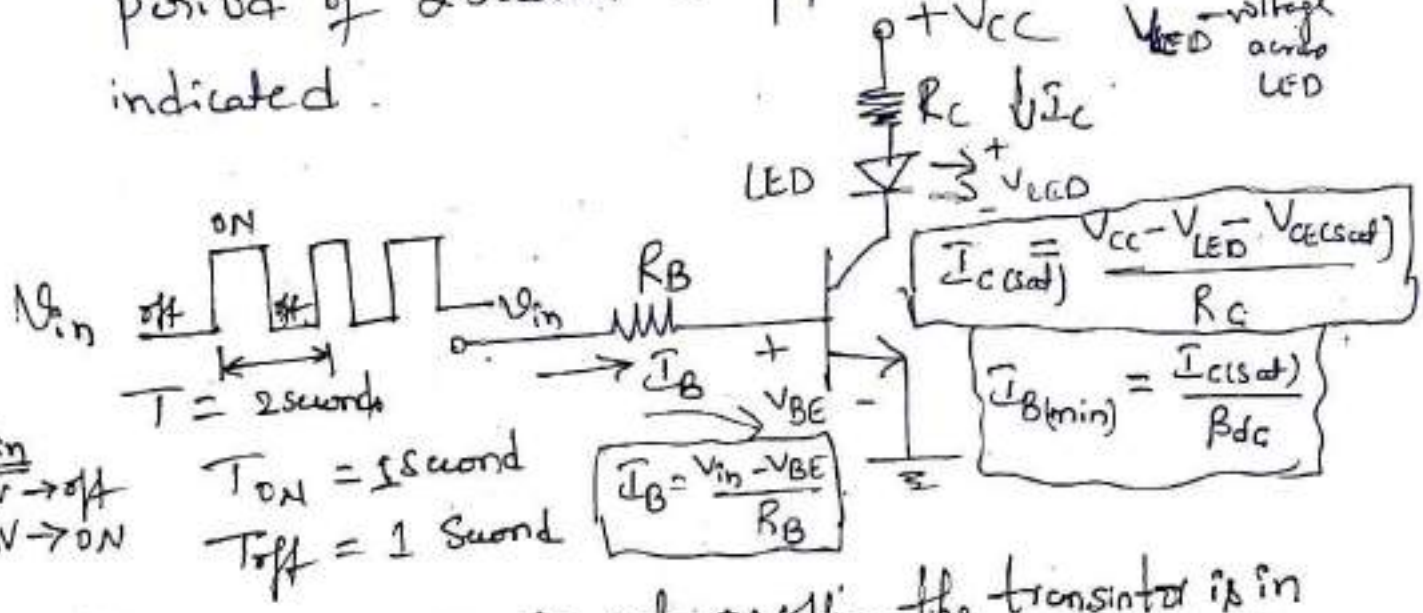
With neat circuit diagram explain how transistor can be used to switch an LED ON/OFF and give the necessary equation. (8 Marks) Dec 2018-Jan 2019.

* The transistor in fig a. is used as a switch to turn the LED ON and OFF.
* for Example a square wave input voltage with a period of 2 seconds is applied to the input as indicated.



* the Square wave is at 0Volts, the transistor is in Cut off; and Since there is no collector current, the LED doesnot Emit light.
* When Square wave goes high Level, the transistor Saturates. This forward biases the LED, the and the resulting collector current through the LED causes it to Emit Light. Thus the LED is on for 1 Second and off for 1 Second.

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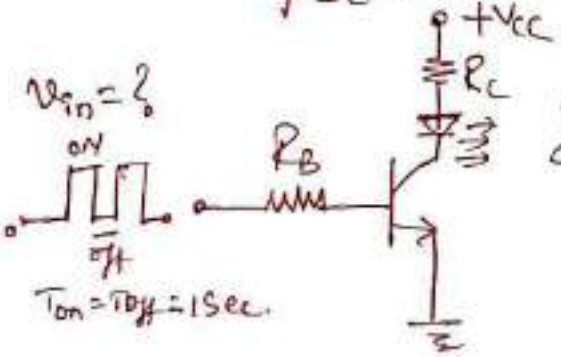
Problem: The LED in fig a. requires 30mA to emit a sufficient level of light. Therefore, the collector current should be approximately 30mA. for the following circuit values, determine the amplitude of the Square wave input voltage necessary to make sure that the transistor saturates. Use double the Minimum value of base Current as a Safety margin to ensure Saturation.

$V_{CC}=9V$, $V_{CE(sat)}=0.3V$, $R_C=220\Omega$, $R_B=3.3k\Omega$

$\beta_{dc}=50$ and $V_{LED}=1.6$ volt.



Soln: $I_{C(sat)} = \frac{V_{CC}-V_{LED}-V_{CE(sat)}}{R_C}$

$= \frac{9-1.6-0.3}{220} = 32.3mA$

$\boxed{I_{C(sat)} = 32.3mA}$

$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{32.3mA}{50} = 646\mu A$

$\boxed{I_{B(min)} = 646\mu A}$

To ensure Saturation, use twice the value of $I_{B(min)}$

i.e $I'_{B(min)} = 2I_{B(min)} = 2(646\mu) = 1.29mA$

KCL at i/p loop. $V_{in} - I_B R_B - V_{BE} = 0$

$\Rightarrow V_{in} = I'_{B_{min}} R_B + V_{BE} = 1.29m(3.3k) + 0.7$

$V_{in} = 4.957$ volts

(or) $\boxed{V_{in} = 4.96 \text{ volts}}$

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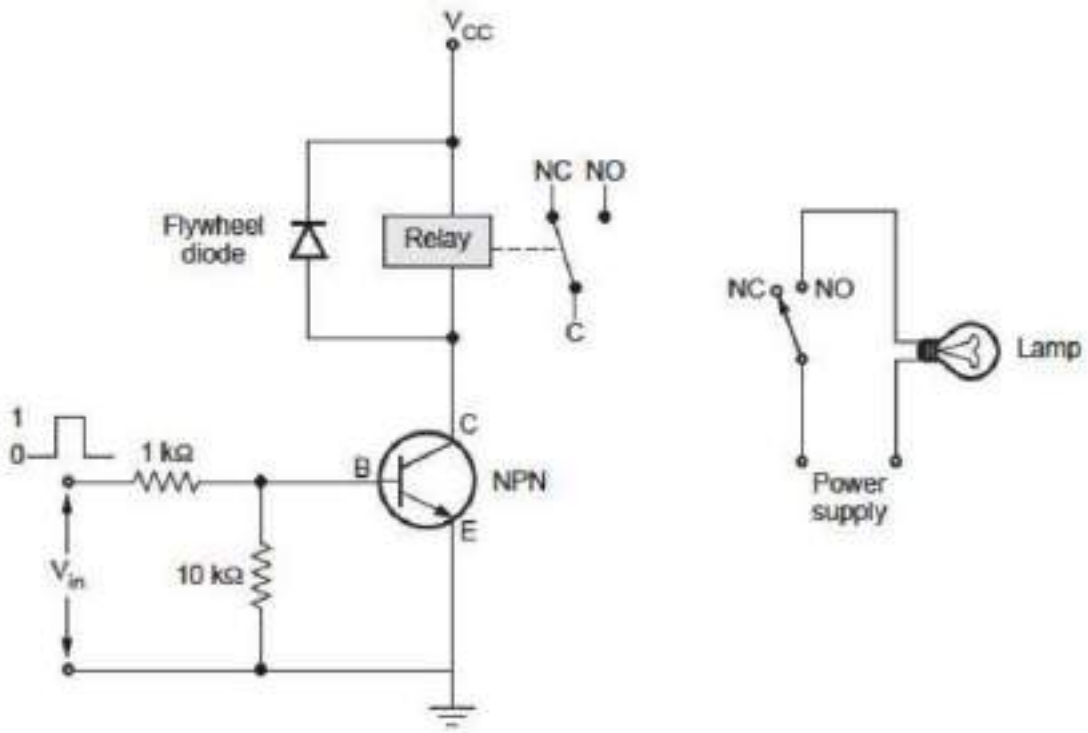
Relay Switch Circuit Using BJT :

Question:

Draw and explain the working of relay switch circuit using BJT to turn OFF/ON lamp.



(a) Typical relay switch circuit (b) Lamp circuit

- Relays are electromechanical devices that use an electromagnet to operate a pair of movable contacts from an open position to a closed position.
- The advantage of relays is that it takes a relatively small amount of power to operate the relay coil.

- Fig. (a) shows a typical relay switch circuit. The circuit has the coil driven by a NPN transistor switch, depending on the input voltage level. When the base voltage of the transistor is zero, the transistor is cut-off and acts as an open switch. As a result no collector current flows and the relay coil is de-energized. In this condition, NC (normally closed) contact remains close and normally open contact remains open.
- When the base voltage of the transistor is sufficient enough to drive the transistor in saturation, transistor acts as a close switch. As a result, collector current flows and the relay coil is energized. In this condition, NC (normally closed) contact gets open and normally open contact gets close.
- We can connect lamp, heater or any other device connecting NO/NC contact in series with power supply to control ON/OFF action. This is illustrated in Fig. (b).

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Topic 2. Feedback Amplifiers

What is a feedback amplifier ? with a necessary diagrams and equation, Briefly explain different types of feedback amplifiers. (06 Marks) MQP-1/(12 Marks) MQP-2.

Soln:- Definition :- The amplifier in which a part of output is sampled and fed back to the input of the amplifier is called feedback amplifier.

* at the input we have two signals :(i) Input signal and (ii) part of the output which is fed back to the input.

Types :- i. positive feedback
ii. Negative feedback.
} This Classification is based on phase of the input and feedback signal.

i. positive feedback :- Both these signals i.e. input signal and feedback signal [part of output signal] are is same phase (in-phase). the feedback is called positive feedback.

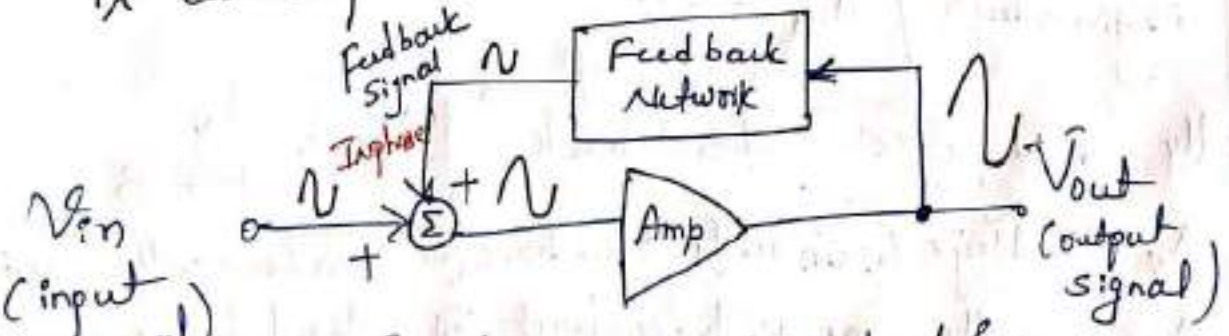

fig:- positive feedback Amplifier

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ii. Negative feedback :- When the input signal and feedback signal are out-of phase, the feedback is called Negative feedback.

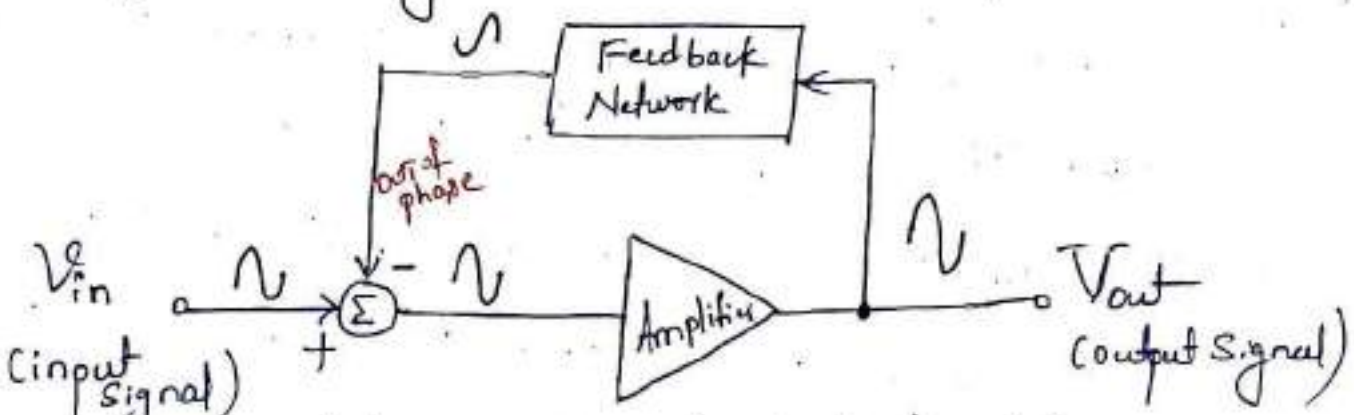

fig b:- Negative feedback Amplifier.

Applications:-

* Use of positive feedback results in oscillations and hence used in oscillators.
* Negative feedback gives stability and hence used in amplifiers.

Voltage Gain :-

* The voltage gain of the positive feedback Amplifier is given by $A_{vf} = \frac{A_v}{1 - A_v\beta}$
* My for Negative feed-back $A_{vf} = \frac{A_v}{1 + A_v\beta}$

A_v – voltage Gain without feedback or open Loop voltage gain.
A_{vf} – voltage gain with feedback or Closed loop gain.
β – feedback factor.

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→ (Covered in previous section).

What is feedback amplifier? what are the properties of negative feedback amplifier ? **(6 Marks) June-July 2019.**

Soln:- Properties of Negative Feedback Amplifiers:-

i. Desensitize the gain.
it brings stability to amplifier by making gain less sensitive to all kind of variations.

ii. Reduce non Linear distortion.
The negative feedback makes the output proportional to the input. i.e reduces non-Linear distortion.

iii. Reduce the effect of Noise.
it minimizes the contribution by unwanted electrical signals. This noise may be generated by ckt components (or) by External interference.

iv. Control the input and Output impedances.
it increases (or) decreases the input and output impedances. This is done by choosing appropriate feedback topology.

v. Extend the Bandwidth of the Amplifier.
By incorporating negative feedback, the bandwidth can be increased.

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Types of Negative Feedback Amplifiers

There are four types of feedback Amplifiers.

i. Voltage Series feedback Amplifier.
ii. Current Series feedback Amplifier.
iii. Voltage Shunt feedback Amplifier.
iv. Current Shunt feedback amplifier.

Parameter	Feedback Topology			
	Voltage Series	Current Series	Voltage Shunt	Current Shunt
Input impedance	increases (↑)	increases (↑)	decreases (↓)	decreases (↓)
Output impedance	decreases (↓)	increases (↑)	decreases (↓)	increases. (↑)

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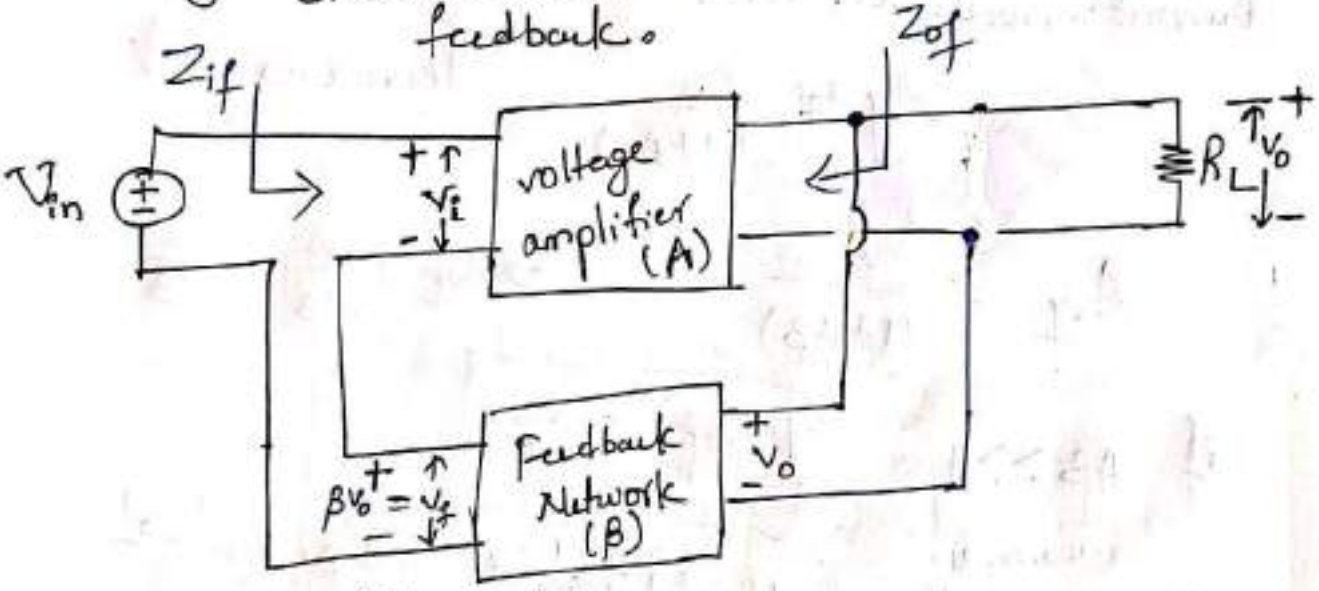
Q.

Explain the voltage series feedback circuit and derive an equation for voltage gain Av with feedback. (4 Marks) Dec 2018-Jan 2019./ (6 Marks) June-July 2019./ (04 Marks) Dec 2019-Jan 2020./ (06 Marks) MQP-1

Soln:- fig. shows the voltage series feedback amplifier circuit. it is also known as series parallel feedback.



$V_f = \beta V_o$

fig:- Voltage Amplifier with voltage series feedback

from fig:- $V_i = V_{in} - V_o\beta$

$V_o = A \cdot V_i = AV_{in} - A\beta V_o$

$\Rightarrow V_o + A\beta V_o = AV_{in}$

the gain with feedback

$$A_{vf} = \frac{V_o}{V_{in}} = \frac{A}{(1+A\beta)}$$ (↓) decreased

obs:- the Amplifier gain reduced by a factor of $(1+A\beta)$

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The input impedance with feedback

$$Z_{if} = Z_i(1+A\beta), \text{ increases. } (\uparrow)$$

Output impedance with feedback,

$$Z_{of} = \frac{Z_o}{(1+A\beta)}, \text{ decreases. } (\downarrow)$$

$$A_{vf} = \frac{A}{(1+A\beta)} \Rightarrow A_{vf} = \frac{A}{A\beta} = \frac{1}{\beta}$$

if $A\beta >> 1$ $\boxed{A_f = \frac{1}{\beta}}$

This Means the feedback amplifier gain is independent of amplifier gain (A). Thus all the distortions like amplitude and frequency distortion do not appear in A_f.

* Even the noise signal, which gets attenuated by feedback.

Any variation in magnitude of A does not appear in A_f. Which means A_f has high gain stability.

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List the advantages of negative feedback in an amplifier. Explain the voltage series feedback amplifier. Show that the gain bandwidth product for a feedback amplifier is constant. **(10 Marks) MQP-3.**

Soln:- Advantages of Negative feedback? -

In negative feedback Amplifier, the gain of the amplifier reduces, however it is still used in almost Every amplifier due to its various advantages. that are

i. Gain stability.
ii. Significant extension of Bandwidth.
iii. Varylen distortions.
iv. Decreased output resistance.
v. Stable operating point.
vi. Reduces noise and other interference in amplifier.

all advantages are on cost of reduced gain of amplifier, and hence in negative feedback there is always a trade-off between amplifier gain and other desirable properties.

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Gain and Bandwidth of Feedback Amplifier

The negative feedback reduces the amplifier gain.

i.e $A_{vf} = \frac{A}{(1+A\beta)}$ ← (1)

* fig a. shows the frequency response of an Amplifier with and without feedback.

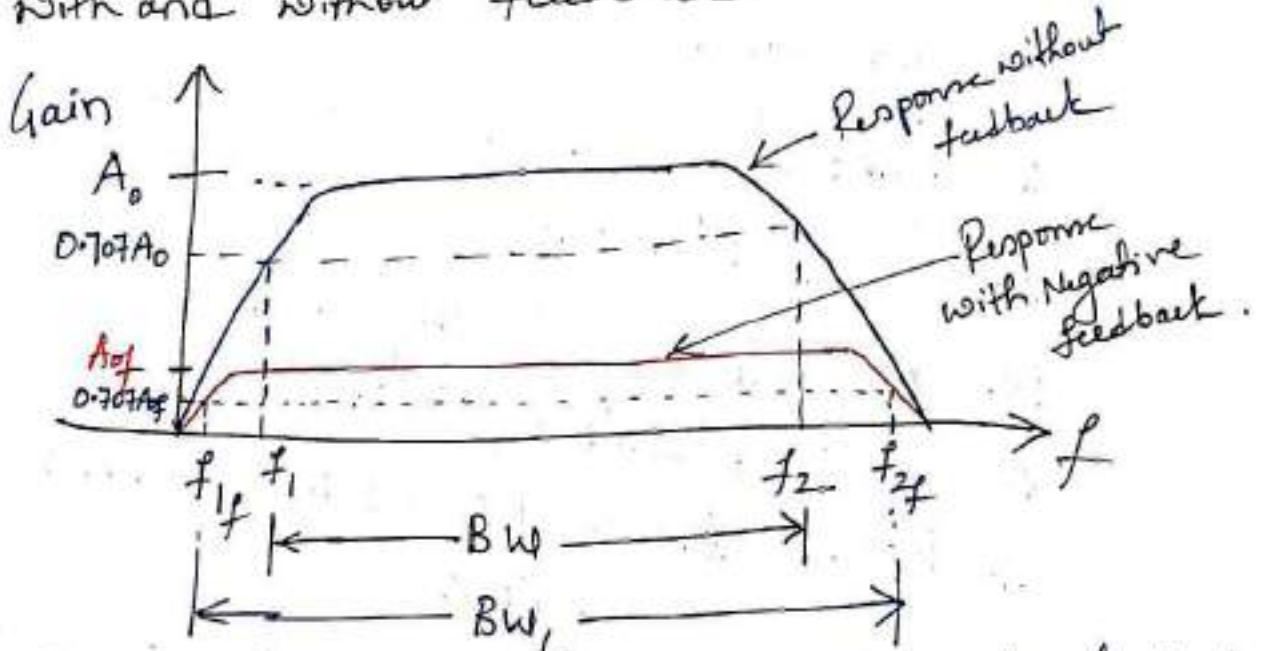

fig:- Effect on A_0 and Bandwidth of negative feedback.

$BW = f_2 - f_1$

Since $f_2 >> f_1$ ∴ $\boxed{BW \simeq f_2}$ Hz

$BW_f = f_{2f} - f_{1f}$

$f_{2f} >> f_{1f}$ ∴ $\boxed{(BW)_f \simeq f_{2f}}$ Hz

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Obs:- i. Since $f_{2f} > f_2$

$\Rightarrow BW_f = (BW)\cdot(1+A_0\beta)$ ← (2)

ii. $\therefore (BW_f) > (BW)$

(BW_f) ↑ Bandwidth with feedback

(BW) ↑ Bandwidth without feedback.

iii. $A_0 \rightarrow$ Gain without feedback

$A_{0f} = \dfrac{A_0}{(1+A_0\beta)}$; → Gain with feedback (reduced)

∴ it can be shown that

$(G\cdot BWP)_{\text{without feedback}} = (G\cdot BWP)_{\text{with feedback}}$

$A_0 \times f_2 = A_{0f} \cdot f_{2f}$

i.e $\boxed{A_0 \cdot f_2 = A_{0f} \cdot f_{2f} = \text{Constant product of gain Bandwidth}}$

Note:- Since B.W with Negative feedback increases by factor $(1+A_0\beta)$ and gain decreases by same factor. ∴ the gain bandwidth product of an amplifier doesn't altered when negative feedback is introduced.

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Gain Stability With Feedback

W.k.t the overall gain with negative feedback is

$$A_f = \frac{A}{1+A\beta} \leftarrow (1)$$

differentiating on both sides

$$\frac{dA_f}{A_f} = \frac{1}{(1+A\beta)} \cdot \frac{dA}{A}$$

for $A\beta >> 1$

$$\boxed{\frac{dA_f}{A_f} \simeq \frac{1}{A\beta} \cdot \frac{dA}{A}} \simeq \frac{1}{A\beta}\left(\frac{dA}{A}\right)$$

This shows that relative change in (dA/A) in the basic amplifier gain reduced by factor $A\beta$ in the relative change (dA_f/A_f) in the overall gain of the feedback Amplifier.

B10.

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An amplifier has a high frequency response described by $A = \frac{A_0}{1+(\frac{j\omega}{\omega_2})}$. Where in $A_0=1000$, $\omega_2=10^4$ rad/sec. Find the feedback factor which will raise the upper corner frequency ω_2 to 10^5 Hz. What is the corresponding gain of the amplifier? Find also the gain bandwidth product in this case. **(04 Marks)**
MQP-3.

Soln:- Given $A = \frac{A_0}{1+(j\omega/\omega_2)}$

$A_0 = 1000$, $\omega_2 = 10^4$ $\Rightarrow$ $\omega_{2(new)} = 10^5$

the gain with feedback

$$A_{(new)} = \frac{A_0}{1+A_0\beta} \quad \leftarrow (1)$$

and the frequency, with feedback

$$\omega_{2(new)} = \omega_2 (1+A_0\beta) \quad \leftarrow (2)$$

find feedback factor $\beta = ?$

given that $\omega_2 \rightarrow \omega_{2(new)}$

using eq^n (2)

$$10^5 = 10^4 [1+1000(\beta)]$$

$$10 = 1+1000\beta$$

$$\Rightarrow \beta = \frac{9}{1000} = 0.009$$

$$\boxed{\beta = 0.009}$$

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the feedback factor $\beta = 0.009$; which will raise the upper corner frequency (ω_2) to 10^5 rad/sec.

W.k.t

$\Rightarrow$ Gain-bandwidth product with and without feedback are constant.

Gain BW p without feedback $= \omega_2 A_0$

$$\boxed{\omega_2 \cdot A_0 = 10^4 \times 1000 = 10^7} \leftarrow (a)$$

GBWP with feedback

$$\omega_{2(new)} \cdot A_{(new)} = ?$$

using eq^n (1) $\quad A_{(new)} = \dfrac{A_0}{1 + A_0\beta} = \dfrac{1000}{1 + 1000(0.009)}$

$$A_{(new)} = \frac{A_0}{10} = \frac{1000}{10} = 100$$

$\boxed{A_{new} = 100}$ obs:- Gain with feedback is reduced.

$\therefore$ GBWP with feedback

$$\boxed{\omega_{2(new)} \cdot A_{(new)} = 10^5 \times 100 = 10^7} \leftarrow (b).$$

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Comparison between Positive and Negative Feedback Amplifiers:

Sr. No.	Parameter	Positive Feedback	Negative Feedback
1.	Phase shift between feedback signal and input signal	0 or 360°	180°
2.	Feedback signal and input signals	Are in phase	Are out of phase
3.	Input voltage	Increases	Decreases
4.	Output voltage	Increases	Decreases
5.	Voltage gain	Increases	Decreases
6.	Distortion	Increases	Decreases
7.	Stability	Decreases	Increases
8.	Application	Used in oscillators and Schmitt triggers	Used in amplifiers

---

➢ ***State the effect of voltage series feedback on input impedance, output impedance and gain of the amplifier.***

- Table shows the changes in the input impedance, output impedance and gain of the voltage series amplifier with negative feedback.

Parameter	Voltage series feed back		Change with -ve feedback
	Without feedback	With feedback	
Input impedance	Z_i	$Z_{if} = Z_i(1+A\beta)$	Increases
output impedance	Z_o	$Z_{of} = Z_o/(1+A\beta)$	Decreases
voltage gain	A_v	$A_{vf} = A_v/(1+A\beta)$	Decreases

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Explain the Barkhausen's criteria for oscillations. **(06 Marks) MQP-1**

Oscillator :-

* Oscillator is an energy converter. it receives dc energy and changes it into ac energy of desired frequency. The frequency of oscillations depends upon the constants of the device.

Def^n:- The composite electric circuit anociated with an active device when used to produce an alternating current is called an oscillator circuit.

* An oscillator is an amplifier which uses a positive feedback. and without any external input signal, generates an output wavform at a desired frequency.

Applications:-

i. In Communication Syetem. to generate Radiowaves.
ii. Tone generator.
iii. generate clock signal to control speed of digital Syetem.
iv. Used as a Local oscillator to transform the RF signals to IF signals in a receiver.

Condition for oscillation / Barkhausen Cond^n for oscillation :-

* Fig. shows the schematic of a basic oscillator circuit.

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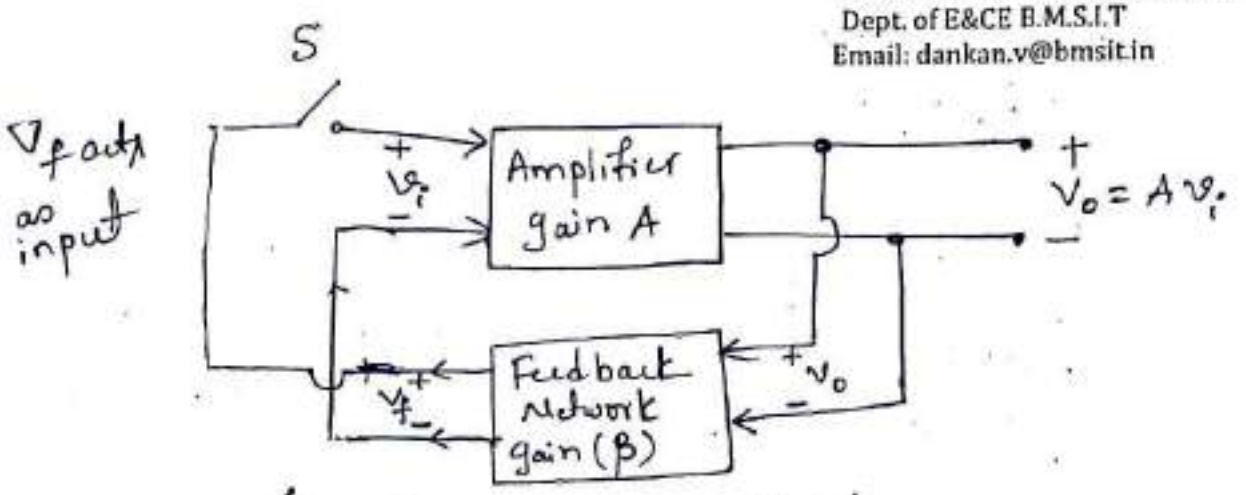

fig. Basic oscillator circuit.

* The feedback signal V_f drives the circuit hence $V_i = 0$ i.e No External input is used.

* for the feedback amplifier shown in fig. the gain with the feedback is given by

$$A_f = \frac{V_o}{V_{in}} = \frac{A}{1+A\beta}$$

* when $V_{in} = 0$, the gain tends to infinity and

$1 + A\beta = 0$ for gain to be infinite.

$$A\beta = -1 + j0 = 1 \angle -180^\circ$$

Under this condition, $V_i = 0$ and V_f drives the circuit into oscillations.

The condition $A\beta = -1$ is called Barkhausen Criteria for oscillation.

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* For positive feedback, the $\angle A\beta = -180°$ and the phase shift introduced by amplifier must be $-180°$. Thus the total phase shift around the Loop is $-360°$ (or) $0°$ for positive feedback.

note :- Barkhausen Criterion.

* The total phase shift around a Loop is $0°$ @ $360°$.
* The magnitude of the product of the open Loop gain of the amplifier (A) and feedback factor (β) is unity. i.e $|A\beta| = 1$. and $\angle A\beta = -180°$.

* When Switch 'S' is closed, Small noise voltage begins to buildup and with $|A\beta|$ slightly greater than 1, the oscillation start growing. Then circuit adjusts itself to get $|A\beta| = 1$ to produce Sustained oscillations. [i.e Constant Amplitude and frequency of oscillations].

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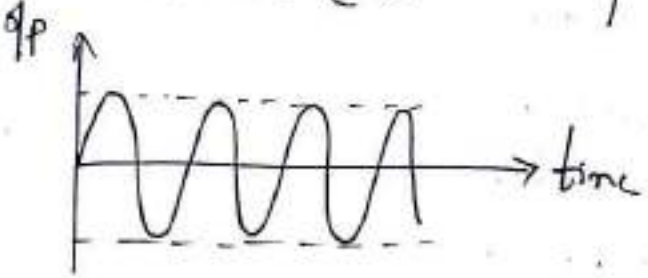
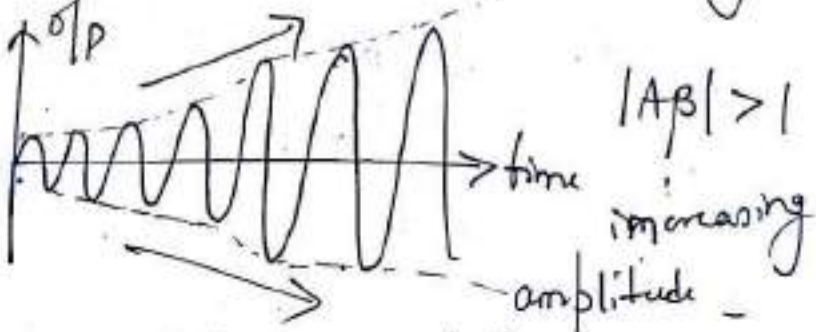
Effect of $|A\beta|$ on Oscillations

* When total phase shift around a loop is 0° (or) 360° and $|A\beta| = 1$, then the output oscillates with constant frequency and amplitude. Such oscillations are called Sustained oscillations (or) Undamped oscillations.



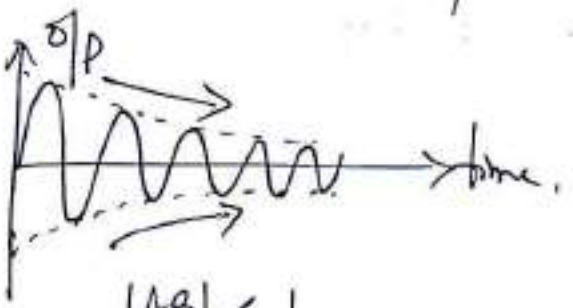
$|A\beta| = 1$
undamped (or)
Sustained oscillation.

* for $|A\beta| > 1$. the oscillations are of increasing amplitude.



$|A\beta| > 1$
increasing

* for $|A\beta| < 1$, the oscillations are of decreasing amplitude.



$|A\beta| < 1$
decreasing amplitude.

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Classification of oscillators

i. Based on operating principle.
   - → Negative resistance effect oscillators.
   - → Feedback oscillators.

ii. Based on Waveforms.
   - → Sinusoidal oscillations.
   - → Non-sinusoidal oscillations (or)
     Relaxation oscillations.

iii. Based on Frquency generation.
   - → Audio-frquency (AF) oscillators. (20Hz to 20kHz)
   - → Radio frequency (RF) oscillators (20kHz – 30MHz)
   - → Ultra-High frquency (UHF) oscillators (300MHz – 3GHz)
   - → Microwave oscillators (3GHz – 30GHz).

iv. According to the Circuit Employed.
   - → LC Oscillators
   - → R.C oscillators.

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R-C phase shift oscillator.

Topic 3. Oscillators

Explain RC phase-shift oscillator with circuit diagram and necessary equations. (8 Marks) Dec 2018-Jan 2019/ (08 Marks) Dec 2019-Jan 2020./ (06 Marks) MQP-1/(06 Marks) MQP-3.

Soln:- * The RC phase shift oscillator uses three RC sections in its feedback path.

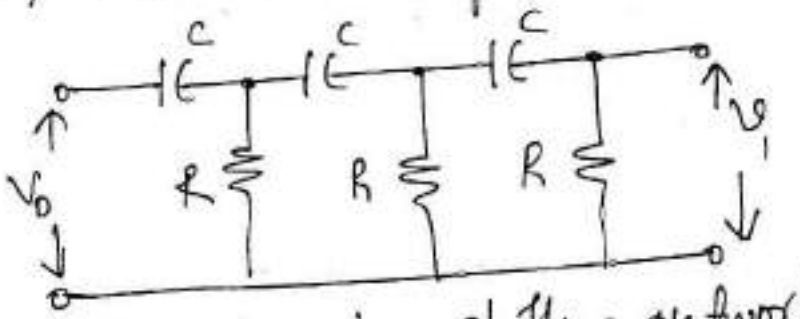

fig a. RC phase shifting network.

* Each RC section produces 60° phase shift hence the total phase shift introduced by the feedback path is

$3 \times 60° = 180°$.

* To satisfy the Barkhausen Criteria, the amplifier path must introduce 180° phase shift in the forward path. Thus total phase shift around the loop becomes 360°.

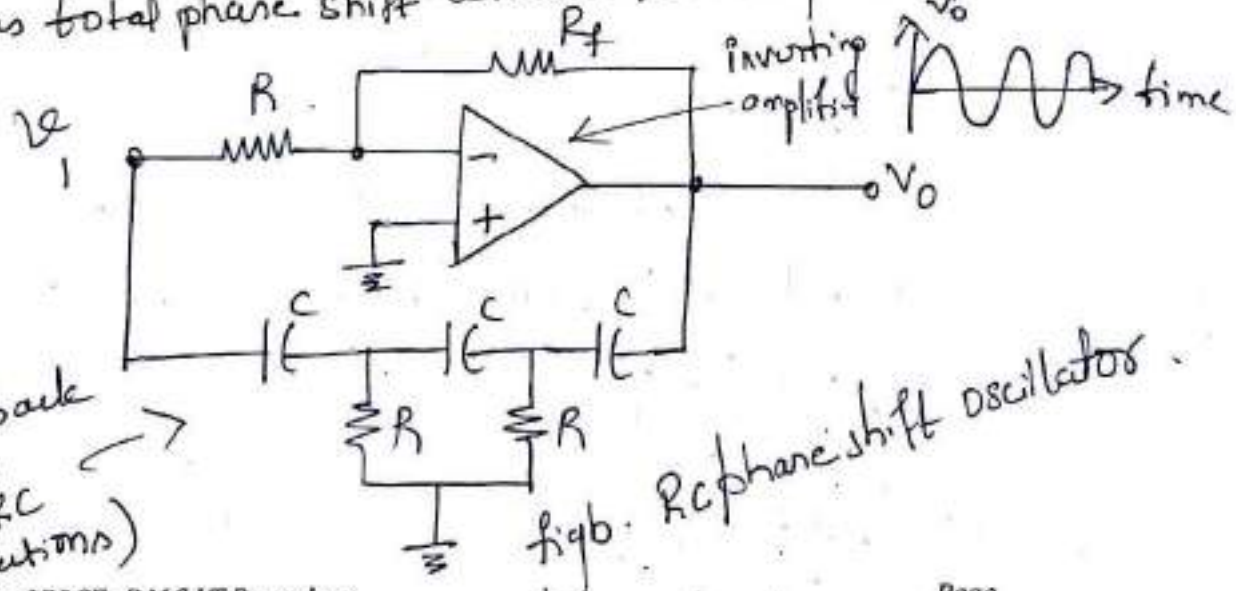

fig b. RC phase shift oscillator.

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* The op-amp (operational amplifier) in the inverting mode is used as an amplifier in the forward path to produce 180° phase shift.
* The output of the amplifier is given to the feedback network while the output of the feedback network drives the amplifier.

the feedback factor $\beta = \frac{V_1(j\omega)}{V_0(j\omega)}$

* The frequency of oscillations is given by

$$\omega_0 = \frac{1}{RC\sqrt{6}} \text{ r/sec} \quad (\omega) \qquad f_0 = \frac{1}{2\pi RC\sqrt{6}} \text{ Hz}$$

* the feedback path gain

$\beta(\omega_0) = -\frac{1}{29}$; 180° phase shift.

$|\beta| = \frac{1}{29}$ and feedback path introduces 180° phase shift.

* To Satisfy Barkhausen condition $|A\beta| = 1$ hence $|A| = \frac{1}{|\beta|} = 29$. Thus the gain of opamp circuit must be 29 to have the oscillations according to Barkhausen Cond^n.
* For inverting amplifier using op-amp the gain is $A = -R_f/R$

$A\beta = \frac{-1}{29}\left(\frac{-R_f}{R}\right)$, $A\beta = \frac{R_f}{29R} > 1$ by Sk, $|A| = \frac{R_f}{R} = 29$ $\therefore$ $\boxed{R_f \geq 29R}$

* Practically R_f is kept slightly higher than 29R so as to supply the energy loss in the circuit.

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Design a RC Phase shift oscillator for a frequency of 1KHz. Draw the circuit diagram with designed values. (6 Marks) June-July 2019.

Soln: Given $f_0 = 1kHz$.

w.k.t frequency of oscillation of R-C phase shift oscillator is $f_0 = \frac{1}{2\pi RC\sqrt{6}}$ Hz.

Let assume $C = 0.1\mu F$

$$R = \frac{1}{2\pi f C\sqrt{6}} = \frac{1}{2\pi(10^3)(0.1\times10^{-6})(\sqrt{6})}$$

$$R = 649.747 \simeq 650\Omega$$

$\therefore$ $\boxed{R = 650\Omega}$ & $\boxed{C = 0.1\mu F}$

and $R_f/R = 29 \Rightarrow R_f = 29R = 29(650)$

$$\boxed{R_f = 18.85k\Omega}$$

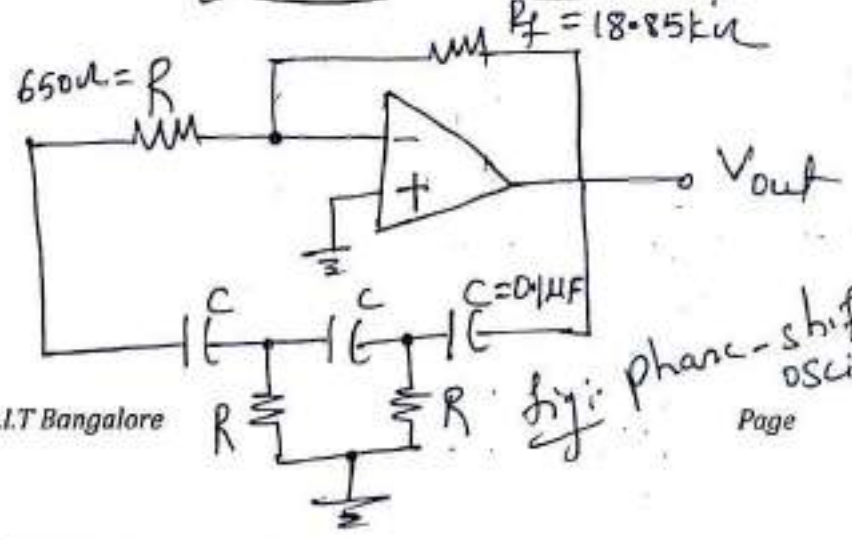

Fig: Phase-shift oscillator.

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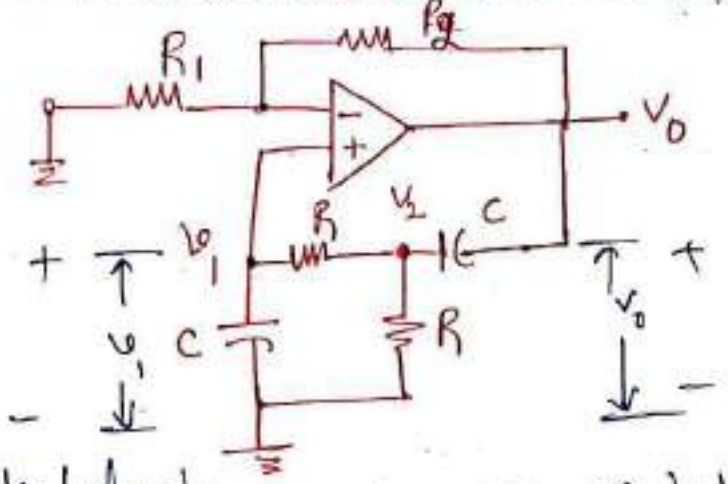
Question: For the feedback ckt shown in fig. determine the condition for oscillation and the oscillation frequency.



Soln:- KCL at node 2 $\quad j\omega C(V_2 - V_0) + \frac{V_2}{R} + \frac{V_2 - V_1}{R} = 0 \leftarrow (1)$

at node 1. $\quad \frac{V_1 - V_2}{R} + j\omega C V_1 = 0 \quad \leftarrow (2)$

$$V_2 = (1 + j\omega RC)V_1 \quad \leftarrow (3)$$

Eq^n (3) in eq^n (1) and re-arranging $\quad \beta = \frac{V_1}{V_0} = \frac{1}{3 + j(\omega RC - 1/\omega RC)}$

for β to be real equate imaginary part (or) j term should be Zero. i.e $\left(\omega RC - \frac{1}{\omega RC}\right) = 0$

$$\boxed{\omega_0 = \frac{1}{RC}} \quad \text{or} \quad \boxed{f_0 = \frac{1}{2\pi RC} \text{ Hz}}$$

then $\beta = +\frac{1}{3}$ (+ve feedback).

forward gain $\quad A = \frac{V_0}{V_1} = 1 + \frac{R_2}{R_1}$

Oscillations to occur. $\quad A\beta = \frac{1}{3}(1 + R_2/R_1) > 1$

$$\frac{R_2}{R_1} > 2 \Rightarrow \boxed{R_2 \geq 2R_1}$$

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Advantages and Disadvantages

➢ ***State the advantages and disadvantages of RC phase shift oscillator.***

- The advantages of R-C phase shift oscillator are,
  1. The circuit is simple to design.
  2. Can produce output over audio frequency range.
  3. Produces sinusoidal output waveform.
  4. It is a fixed frequency oscillator.
  5. Does not require bulky components like transformers and inductors.
  6. Used to produce oscillations of audio frequency range which is 20 Hz to 100 - 200 kHz.

Disadvantages:

- The disadvantages of R-C phase shift oscillator are,
  1. By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible.
  2. The frequency stability is poor due to the changes in the values of various components, due to effect of temperature, aging etc.
  3. As feedback is very small, it is difficult to start the oscillations.

Problem:

A RC phase shift oscillator uses R = 10 kΩ and C = 1 nF. Find its frequency of oscillations.

Sol. : R = 10 kΩ, C = 1 nF

$$\therefore \quad f_o = \frac{1}{2\pi RC\sqrt{6}} = \frac{1}{2\pi \times 10 \times 10^3 \times 1 \times 10^{-9} \times \sqrt{6}}$$

$$= 6.497 \text{ kHz.}$$

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10. Klien Bridge Oscillator

With a neat circuit diagram, explain the working of wein Bridge oscillator. **(6 Marks) June-July 2019./ (08 Marks) Dec 201-Jan 2020.**

Define an oscillator? Derive the equation for Wien bridge oscillator. **(08 Marks) MQP-2**

Soln:- * The Fig. shows Kleinbridge oscillator Circuit.

* The forward path uses an opamp used in noninverting mode. Thus it does not introduce any phase shift.

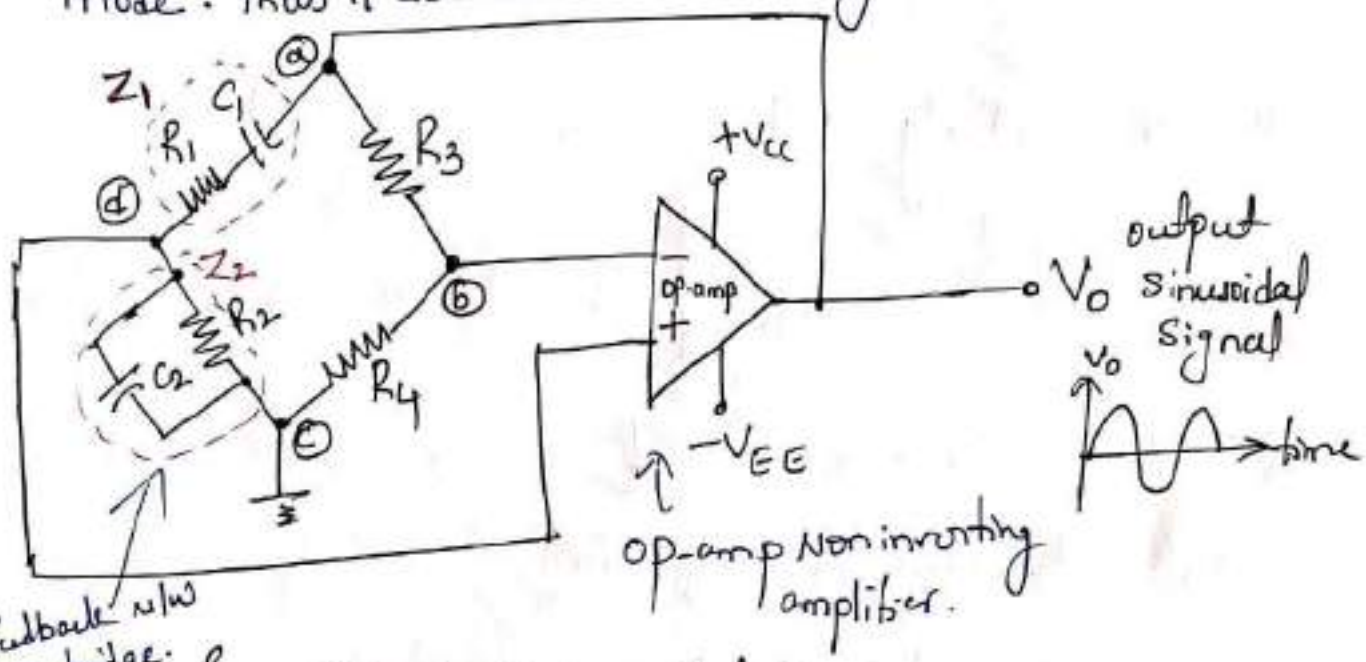

fig a:- Klein bridge oscillator

* Feedback Network uses bridge called Kleinbridge.

* The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called frequency Sensitive arms.

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* The gain of the amplifier is

$$\boxed{A = 1 + \frac{R_3}{R_4}} \leftarrow (1)$$

* The frequency of oscillation is given by

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \text{ rad/sec} \quad \text{(or)} \quad f_0 = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \text{ Hz}.$$

* for Simplicity, choose $R_1 = R_2 = R$ and $C_1 = C_2 = C$.

$$\boxed{f_0 = \frac{1}{2\pi RC}} \text{ Hz} \quad \text{(or)} \quad \boxed{\omega_0 = \frac{1}{RC}} \text{ rad/sec}.$$

* With $R_1 = R_2 = R$ and $C_1 = C_2 = C$ the feedback Network gain $\beta = \frac{1}{3}$ and to satisfy Barkhausen Criteria $A\beta \geq 1$, $A \geq 3$ for the amplifier

$$\left(1 + \frac{R_3}{R_4}\right) \geq 3 \quad \text{i.e} \quad \boxed{R_3 \geq 2R_4}$$

* Satisfying both the Barkhausen Conditions - the Circuit works as an oscillator.

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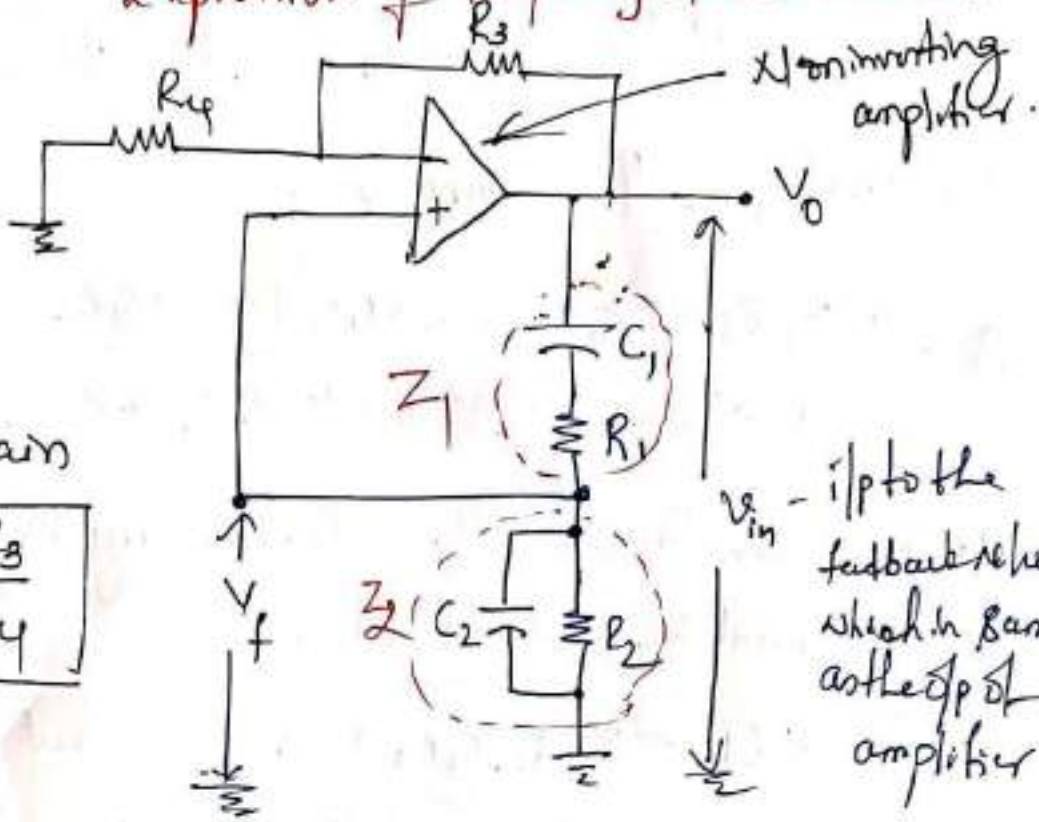
Wienbridge Oscillator

Expression of frequency of oscillation.



Amplifier gain

$$A = 1 + \frac{R_3}{R_4}$$

β - feedback n/w gain $\beta = \frac{v_f}{v_{in}}$

using VDR $v_f = \frac{v_{in}}{(Z_1+Z_2)} \cdot Z_2$

$$\beta = \frac{v_f}{v_{in}} = \frac{Z_2}{Z_1+Z_2}.$$

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{(jR_1C_1\omega + 1)}{j\omega C_1}$$

$$Z_2 = R_2 \parallel \left(\frac{1}{j\omega C_2}\right) = \frac{R_2 \times 1/j\omega C_2}{R_2 + \frac{1}{j\omega C_2}} = \frac{R_2}{1 + j\omega C_2 R_2}$$

C11

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$$\beta = \frac{Z_2}{Z_1+Z_2} = \frac{j\omega R_2 C_1}{(1-\omega^2 R_1 R_2 C_1 C_2) + j\omega(R_1C_1 + R_2C_2 + R_2C_1)}$$

Rationalizing and Simplifying.

$$\beta = \frac{\omega^2 C_1 R_2 (R_1C_1 + R_2C_2 + C_1R_2) + j\omega C_1 R_2 (1-\omega^2 R_1 R_2 C_1 C_2)}{(1-\omega^2 R_1 R_2 C_1 C_2)^2 + \omega^2 (R_1C_1 + R_2C_2 + C_1R_2)^2}$$

To get Zero phase shift, the imaginary part of above eq^n must be equal to Zero.

$\therefore \omega(1-\omega^2 R_1 R_2 C_1 C_2) = 0$, but $\omega \neq 0$

$\therefore \omega^2 R_1 R_2 C_1 C_2 = 1 \Rightarrow \omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$

$$\boxed{\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}} \text{ rad/sec.}$$

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}} \text{ Hz}$$

frquency of oscillation of Wienbridge oscillator.

In practice $R_1 = R_2 = R$, $C_1 = C_2 = C$.

$$\therefore \boxed{f = \frac{1}{2\pi RC}} \text{ Hz}$$

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The frequency sensitivity arms of the wein bridge oscillator uses C1=C2=0.01μF and R1=10KΩ while R2 is kept variable. The frequency is to be varied from 10K Hz to 50K Hz by varying R2. Find the minimum and maximum values of R2. **(04 Marks) MQP-3.**

Soln:- frequency of oscillation of Wein bridge oscillator is

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \text{ Hz} \quad \leftarrow (1)$$

given $C_1 = C_2 = 0.01\mu F = C$.

and $R_1 = 10K\Omega$. R_2 (variable)

from eq^n (1) $f \propto 1/R$.

for $f = 10kHz \Rightarrow R_2(max)$ Maximum

$f = 50kHz \Rightarrow R_2(min)$ - Minimum.

$$f = \frac{1}{2\pi C\sqrt{R_1}\cdot\sqrt{R_2}}$$

use $f = 10kHz$.

$$\sqrt{R_2} = \frac{1}{2\pi C\sqrt{R_1}\cdot f} = \frac{1}{2\pi \times 0.01\times10^{-6}\times10\times10^{3}\times\sqrt{(10\times10^{3})}}$$

$$\sqrt{R_2} = \frac{1}{0.062831853} = 15.9154.$$

$$\boxed{R_2 = 253.302\Omega} = 253.302\Omega$$

(Maximum)

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using $f = 50kHz$

$$\sqrt{R_2} = \frac{1}{2\pi C \sqrt{R_1} f} = \frac{1}{2\pi \times 0.01 \times 10^{-6} \times 50 \times 10^{3} \times \sqrt{10 \times 10^{3}}}$$

$$\sqrt{R_2} = \frac{1}{0.314159} = 3.1830$$

$$\boxed{R_2 = 10.1321\ \Omega} \quad (\text{Minimum})$$

$R_{2(min)} = 10.1321\ \Omega$

$R_{2(max)} = 253.302\ \Omega$.

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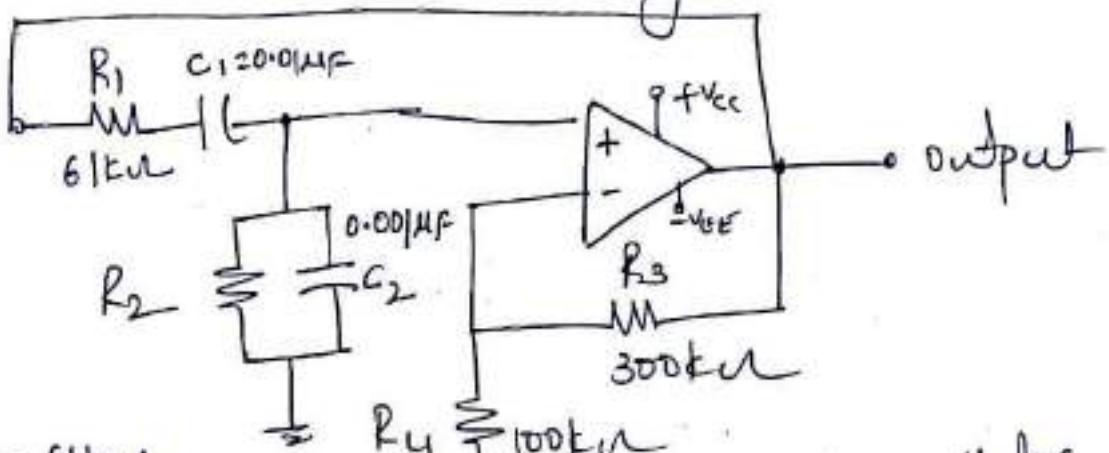
Question.

Calculate the resonant frequency of the Wien bridge oscillator shown in fig.



i. $R_2 = 61k\Omega$

ii. $R_2 = 51k\Omega$.

fig. Wienbridge oscillator.

Soln:- $f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$ Hz.

(i). $R_1 = R_2 = 61k\Omega$, $C_1 = C_2 = C = 0.01\mu F$.

$$f = \frac{1}{2\pi R \cdot C} = \frac{1}{2\pi \times 61K \times 0.01\mu}$$

$$\boxed{f = 260.9 Hz}$$

ii. $R_2 = 51k\Omega$. $f = \frac{1}{2\pi C\sqrt{R_1 R_2}} = \frac{1}{2\pi \times 0.01\mu\sqrt{61k \times 51k}}$

$$\boxed{f = 285.349 Hz}$$

Obs $R_2 \downarrow \Rightarrow f \uparrow$

CIS

Question: Design the RC elements of a Wein bridge oscillator for operation at $f_0 = 10kHz$.

Soln:

$A_v = \left(\frac{R_3}{R_4} + 1\right)$ and $R_3 \geq 2R_4$

$\therefore$ choose $R_4 = 100k\Omega$

and $R_3 = 300k\Omega$.

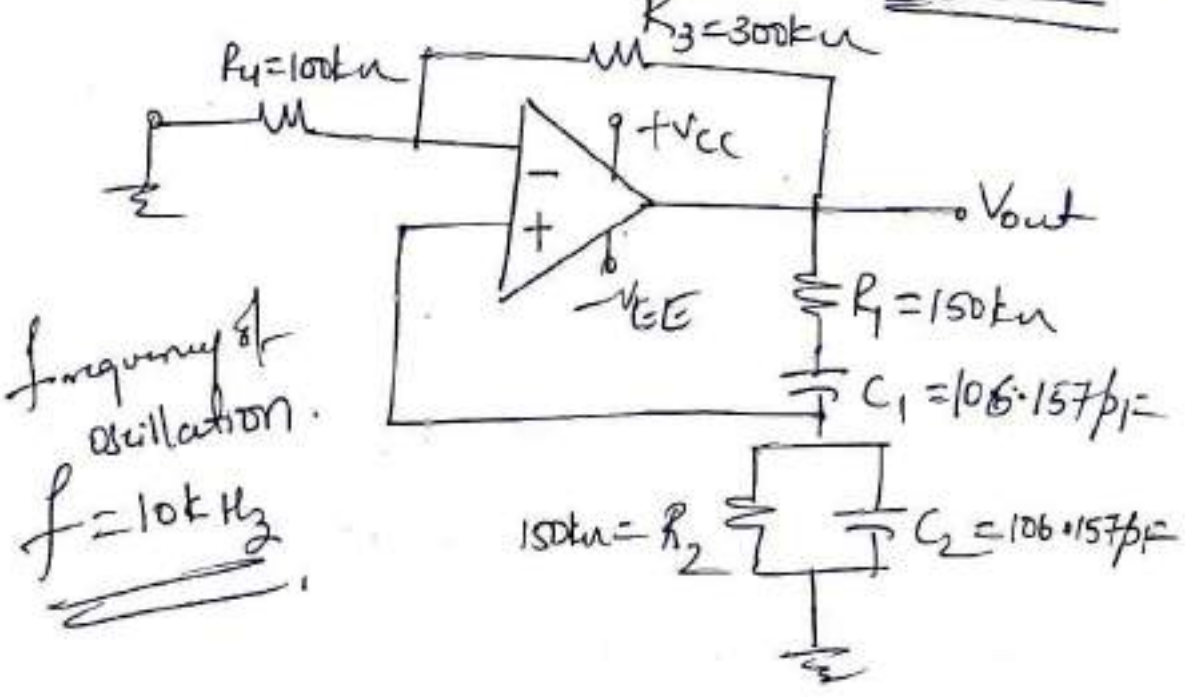
i.e $\frac{R_3}{R_4} > 2$ for oscillation to take place.

given $f = 10kHz$.

choose $R = 150k\Omega$ (i.e $R_1 = R_2 = R = 150k\Omega$)

find $C = \frac{1}{2\pi f \cdot R} = \frac{1}{2\pi \times 10 \times 10^3 \times 150 \times 10^3}$

$C = 106.157pF$ i.e $C_1 = C_2 = C = 106.15pF$



frequency of oscillation.

$f = 10kHz$.

G6

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Advantages and Disadvantages of Wien Bridge Oscillator:

Advantages and Disadvantages

➢ ***State the advantages and disadvantages of Wien bridge oscillator.***

- **The various advantages** of Wien bridge oscillator are,
  1. By varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be obtained.
  2. The perfect sine wave output is possible.
  3. It is useful for audio frequency range i.e. 20 Hz to 100 kHz.
  4. Very useful in laboratory signal generators.
  5. Gives high frequency stability.
  6. Easy from design point of view and gives constant output.

- **The disadvantages** of Wien bridge oscillators are,
  1. The maximum frequency output is limited.
  2. It uses large number of components other than op-amp.
  3. Can not be used to generate high frequencies.

Problems:

Ex. *Determine the component values for Wien bridge oscillator used to obtain the frequency of 12 kHz.*

Sol. : $f = 12\ \text{kHz}, R_1 = R_2 = R,$

$C_1 = C_2 = C$

$\therefore \quad f = \frac{1}{2\pi RC}$ i.e. $12\times10^3 = \frac{1}{2\pi RC}$

$\therefore \quad RC = 1.3263\times10^{-5}$

Choose $C = \mathbf{0.001\ \mu F}$

i.e. $R = \frac{1.3263\times10^{-5}}{0.001\times10^{-6}}$

$\therefore \quad R = \mathbf{13.26\ k\Omega}$

For $A \geq 3$, $R_3 \geq 2R_4$

Choose $R_4 = \mathbf{100\ k\Omega}$ i.e. $R_3 \geq 200\ \text{k}\Omega$

Choose $R_3 = \mathbf{270\ k\Omega}$.

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Ex. *Determine the frequency of the Wien-bridge oscillator using* $R = 5.1\ k\Omega$ *and* $C = 0.001\ \mu F$.

Sol. : Frequency of oscillation for Wien-bridge oscillator is given by,

$$f = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi \times 5.1\,k\Omega \times 0.001\,\mu F}$$

$$= 31206.8\ Hz = \mathbf{31.2068\ kHz}$$

Comparison between RC phase shift and Wien Bridge Oscillators:

Sr. No.	RC phase shift oscillator	Wien bridge oscillator
1.	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
2.	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
3.	An amplifier stage introduces 180° phase shift.	An amplifier stage does not introduce any phase shift.
4.	The frequency of oscillations is, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is, $f = \frac{1}{2\pi RC}$
5.	The amplifier stage gain condition is, $\lvert A\rvert \geq 29$	The amplifier stage gain condition is, $\lvert A\rvert \geq 3$
6.	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

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THE IC 555 TIMER

* The 555 timer IC is an integrated circuit used in a variety of timer, pulse generation and oscillation applications.
* 555 is called so because of its internal circuit. There are three 5k Ω resistors used in the IC and hence the name 555. The resistors are connected in series and are used as voltage dividers.
* Pin diagram.

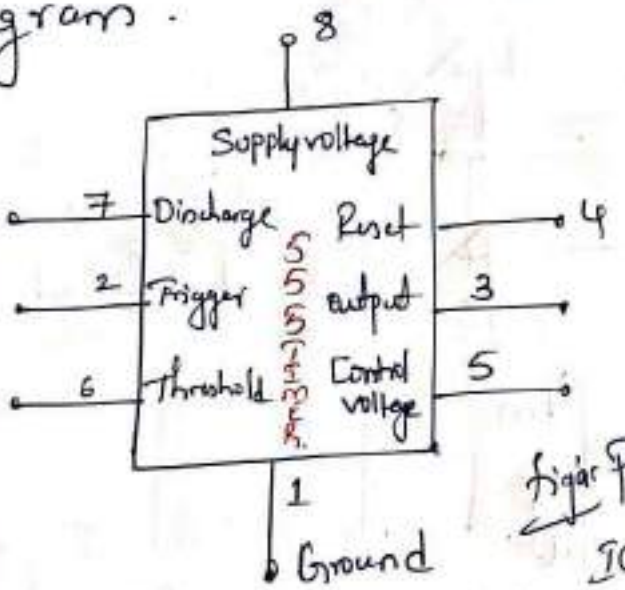

fig: Pin diagram of IC-555

* The detailed (or) internal Circuitry of 555 timer is shown in fig b. it comprises
  i. Two opamp comparators set $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively.
  ii. The three resistor circuit, to obtain voltage $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ to set the comparator.

d)

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* The comparator's output sets (or) resets the Flipflop (F/F) which feeds the output stage.

The F/F operates as

R=1, S=0 , output = 0

R=0, S=1 , output = 1.

* The F/F also operates a transistor which when driven low, discharges a timing capacitor (External).

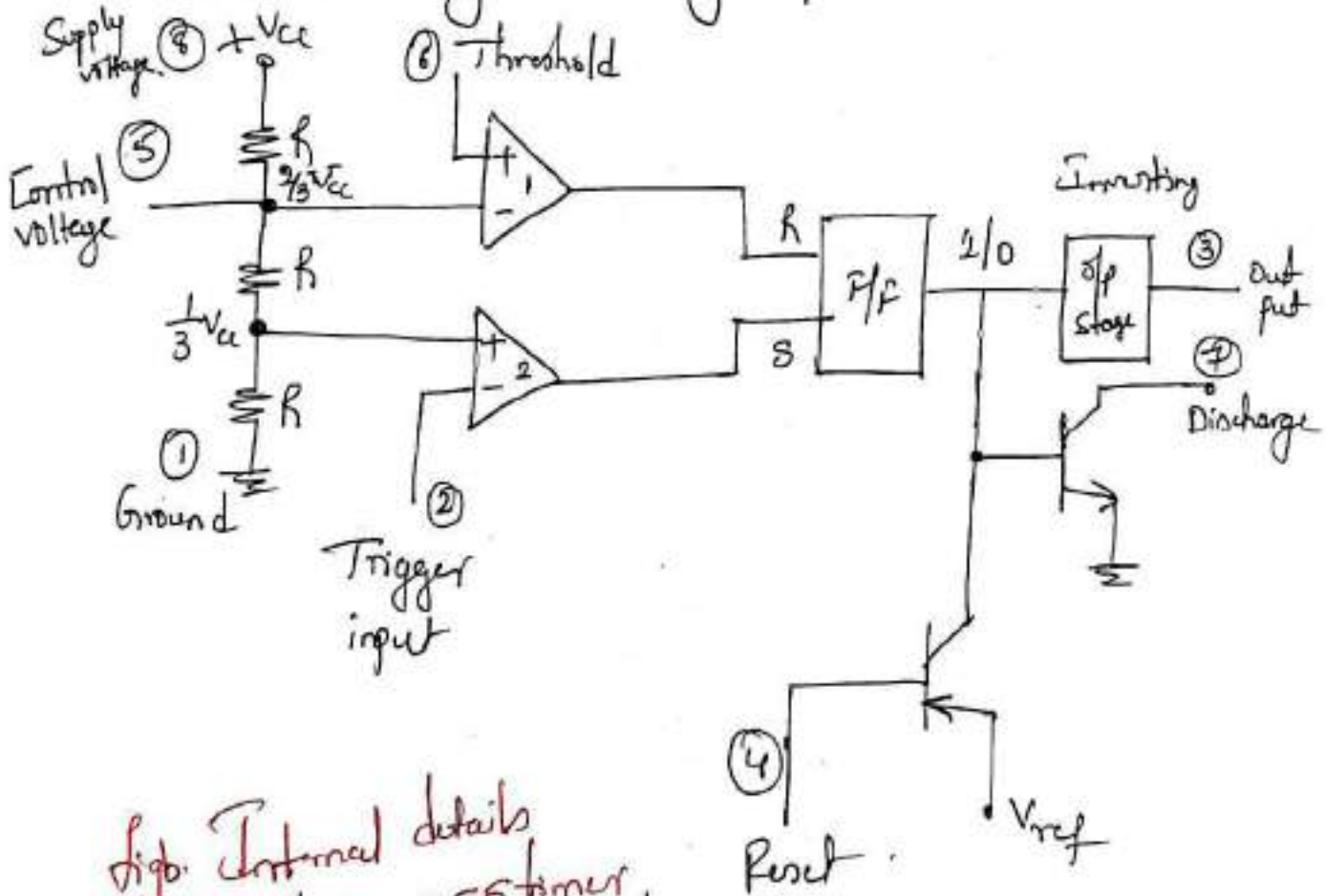

Fig: Internal details of IC-555 timer.

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IC-555 Timer

* IC 555 Timer was introduced in 1970 by 'Signetic Corporation'.
* IC 555 Timer is used for generation of Squarewave, [Asymmetrical and Asymmetrical], Sawtooth Wave and various other applications such as Astable Multivibrator, Monostable Multivibrator etc.
* Circuit diagram :-

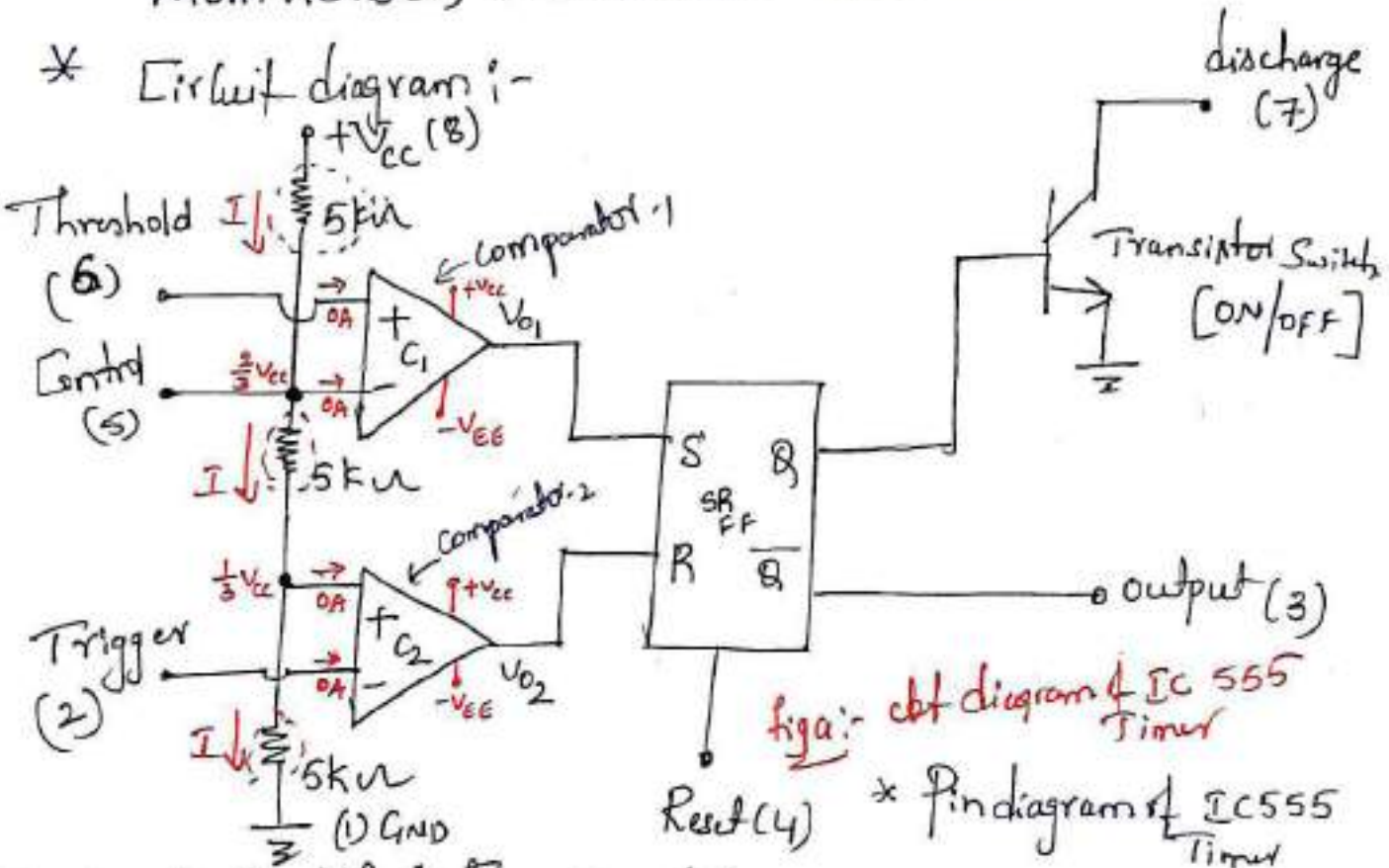

fig a:- ckt diagram of IC 555 Timer

* Pin diagram of IC555 Timer

* Due to these three 5kΩ resistor this IC is know as IC-555 Timer.

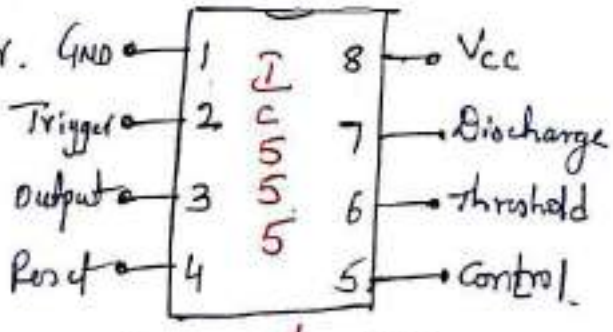

fig b:- pin diagram of IC555 Timer.

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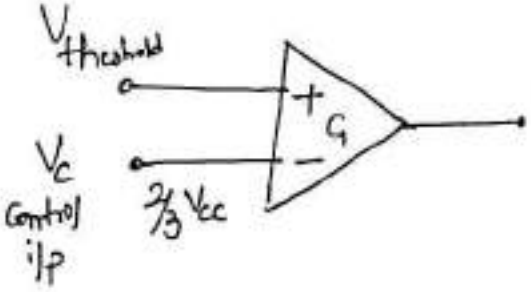
Working :-

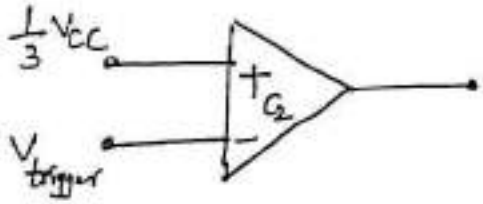
Comparator - 1

$$V_c = \frac{V_{cc}}{3(5k)} \times 2(5k) = \frac{2}{3}V_{cc}$$



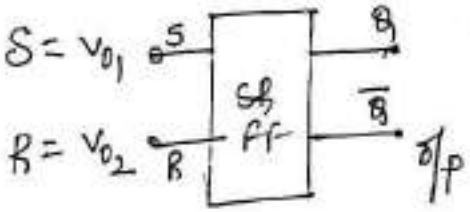
$$V_{o_1} = \begin{cases} +V_{CC} \text{ (logic 1)} ; & V_{th} > \frac{2}{3}V_{cc} \\ -V_{EE} \text{ (logic 0)} ; & V_{th} < \frac{2}{3}V_{cc} \end{cases}$$

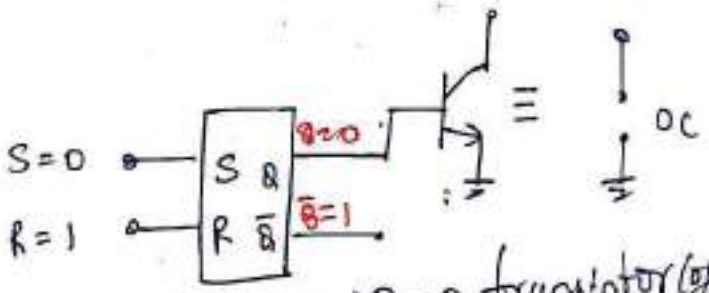
Comparator - 2



$$V_{o_2} = \begin{cases} -V_{EE} \text{ (logic 0)} ; & V_{trig} > \frac{1}{3}V_{cc} \\ +V_{CC} \text{ (logic 1)} ; & V_{trigg} < \frac{1}{3}V_{cc} \end{cases}$$

SR-Flip Flop :

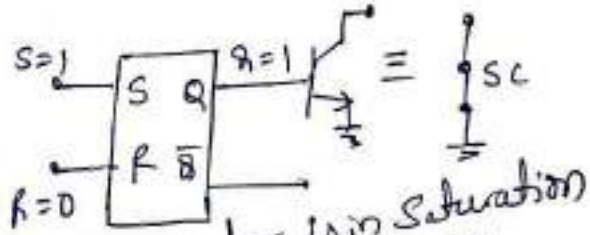




S=0, R=1 ⇒ Q = 0 transistor (off) is in cut-off region ∴ open ckt.

S (V_{o_1})	R (V_{o_2})	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	Q_n	$\bar{Q}_n$	(previous state)
0	1	0	1	Reset
1	0	1	0	Set
1	1	x	x	(not defined)

S=1, R=0 ⇒ Q = 1



Transistor is in Saturation region ∴ (ON) it acts as short circuit.

dy

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Topic 4. 555 Timer

Explain the operation of IC-555 as an Astable oscillator (astable operation) with neat circuit diagram and necessary equation. **(08 Marks) Dec 2018-Jan 2019./ (08 Marks) Dec 2019-Jan 2020./ (08 Marks) MQP-1/ (06 Marks) MQP-3.**

With a neat circuit diagram and waveforms, explain the working of 555 timers as an oscillator. **(8 Marks) June-July 2019.**

Explain how 555 timers can be used as an oscillator. **(06 Marks) MQP-2**

Soln:- Astable Multivibrator is used to generate Squarewave.

Circuit diagram:-

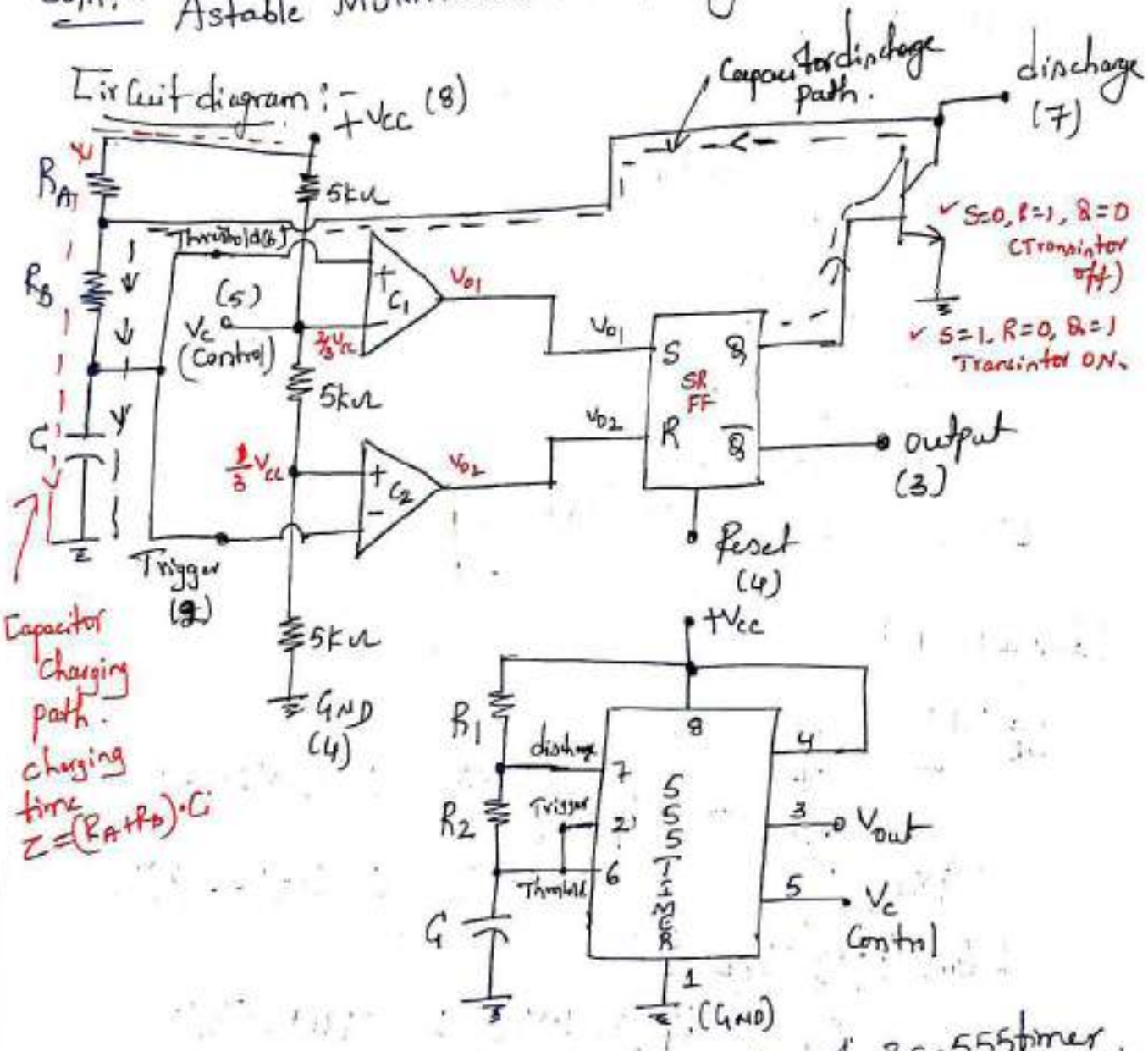

fig:- Astable operation of IC 555 timer.

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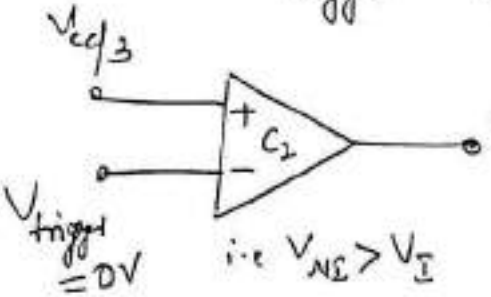
Working:-

assume, $V_c(0^-) = V_c(0+) = 0$ volt

$\therefore V_{trigger} = V_{threshold} = V_c(t) = 0$ volts.

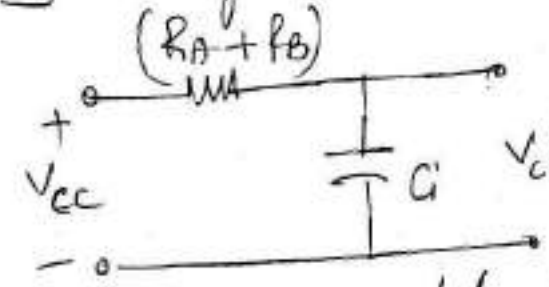


$V_{o_2} = V_{cc}$ (Logic 1)

i.e $V_{NI} > V_I$ i.e $R=1 \Rightarrow Q=0$ ∴ transistor is OFF (acts as open circuit).

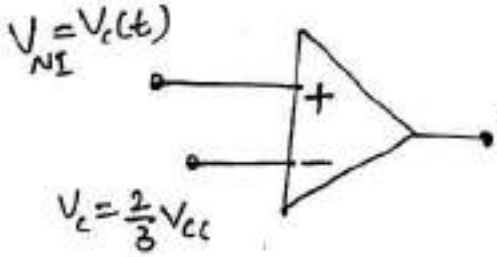
$\Rightarrow$ at $t=0$, the capacitor charging path Exists.

Charging Circuitry



$$V_c(t) = V_{cc}\left[1 - e^{-t/(R_A+R_B)C}\right] \leftarrow (1)$$

Comparator-1



$$V_{o_1} = \begin{cases} +V_{cc} & : V_c(t) > \frac{2}{3}V_{cc} \\ -V_{EE} & : V_c(t) < \frac{2}{3}V_{cc} \end{cases}$$

at time $t=0$, $V_c(t) = V_{cc}$

$\therefore V_{o_1} = +V_{cc}$; $V_c(t) > \frac{2}{3}V_{cc}$

↓ Logic 1

$\therefore \boxed{S = V_{o_1} = 1}$

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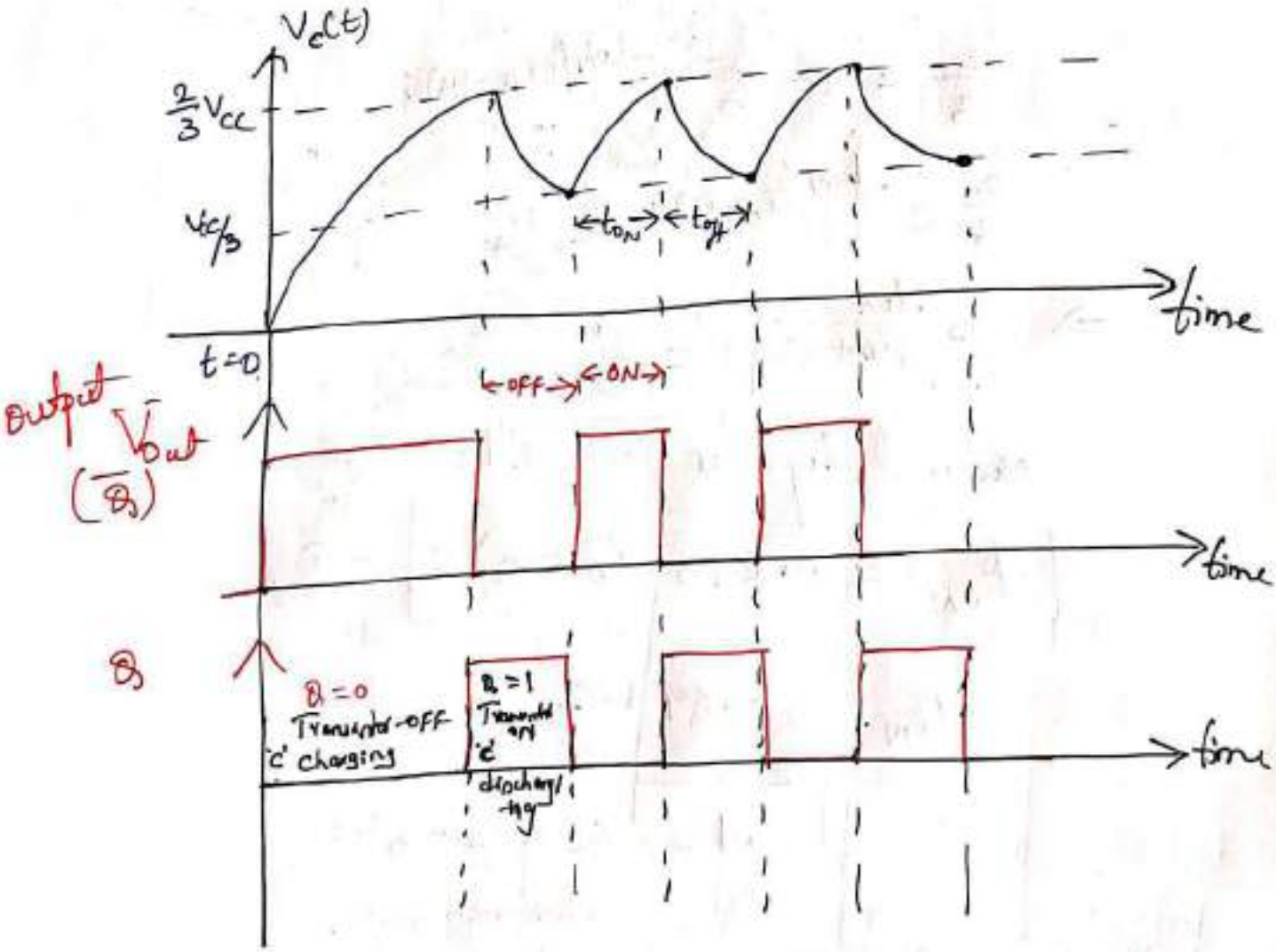
When S = 1, the o/p of SR FF $\bar{Q} = 1$, ⇒ transistor acts as (ON) switch means discharging path exist.

1st charging ⇒ 0 to $\frac{2}{3}V_{cc}$

1st discharging ⇒ $\frac{2}{3}V_{cc}$ to $V_{cc}/3$.

2nd Charging ⇒ $V_{cc}/3$ to $\frac{2}{3}V_{cc}$.

2nd discharging ⇒ $\frac{2}{3}V_{cc}$ to $V_{cc}/3$.



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Calculation of ON Time (T_{ON})

$$V_c(t) = V_c(\infty) + [V_{cc}(0^+) - V_c(\infty)]e^{-t/\tau}$$

$$\tau = (R_A + R_B) \cdot C$$

$$V_c(0^+) = \frac{V_{cc}}{3}$$

$$V_c(\infty) = V_{cc}$$

$$V_c(t = t_{ON}) = V_{cc} + \left[\frac{V_{cc}}{3} - V_{cc}\right] e^{-\frac{t_{ON}}{(R_A+R_B)C}}$$

$$\frac{2}{3}V_{cc} = V_{cc} - \frac{2}{3}V_{cc}\, e^{-t_{ON}/(R_A+R_B)C}$$

$$\frac{2}{3} = 1 - \frac{2}{3} e^{-t_{ON}/(R_A+R_B)C}$$

$$\frac{2}{3} e^{-t_{ON}/(R_A+R_B)C} = 1/3$$

$$\Rightarrow e^{\frac{-t_{ON}}{(R_A+R_B)C}} = \frac{1}{2}$$

Natural log on both side

$$\boxed{t_{ON} = 0.693(R_A+R_B)C} = T_{ON}$$

$$T_{ON} = 0.693 \cdot \tau_c$$

where $\tau_c = (R_A + R_B) \cdot C$

charging time.

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Calculation of off time (T_{off})

$$V_c(t) = V_c(\infty) + [V_c(0+) - V_c(\infty)]\, e^{-t/\tau}$$

$\tau = R_B \cdot C$ (discharging time constant).

$V_c(0+) = \frac{2V_{cc}}{3}$ and $V_c(\infty) = 0$ volts.

2nd

$$\frac{V_{cc}}{3} = 0 + \left(\frac{2}{3}V_{cc} - 0\right) e^{-t_{off}/R_B \cdot C}$$

$$\frac{V_{cc}}{3} = \frac{2}{3}V_{cc} \cdot e^{-t_{off}/R_B \cdot C}$$

$$\frac{1}{2} = e^{-t_{off}/R_B \cdot C}$$

$$\Rightarrow \boxed{t_{off} = 0.693 R_B \cdot C}$$

Total time period (T)

$$T = T_{on} + T_{off}$$

$$= 0.693(R_A + R_B) \cdot C + 0.693 R_B \cdot C$$

$$\boxed{T = 0.693 \cdot C (R_A + 2R_B)}$$ ← Time period of generated square wave

frequency of oscillation $\boxed{f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}}$ Hz

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Duty-cycle:-

$$D = \frac{t_{ON}}{T} = \frac{0.693(R_A+R_B)\cdot C}{0.693(R_A+2R_B)\cdot C}$$

$$\boxed{D = \frac{R_A+R_B}{R_A+2R_B}}$$! Lesthan 50%.

$$\%\ D = \frac{R_A+R_B}{R_A+2R_B} \times 100\%$$

Note:- Duty cycle is independent of capacitor.

d.o.

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Problem1.

For a 555 timer connected as Astable Multivibrator, $R_1 = R_2 = 7.5k\Omega$, $C = 0.1\mu F$, $V_{cc} = 5V$. Calculate the frequency of operation and sketch output waveform.

Soln:-

$$T_{ON} = 0.693 (R_1 + R_2) \cdot C$$

$$= 0.693 (7.5k + 7.5k)(0.1\mu)$$

$$\boxed{T_{ON} = 1.05 \text{ msec}}$$: Capacitor charging time.

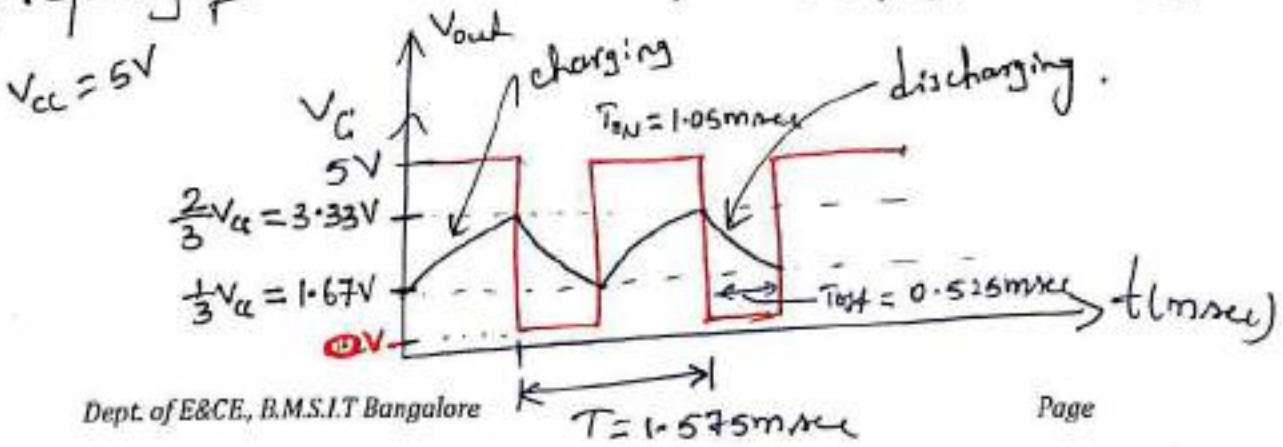
$$T_{off} = 0.693 R_2 C$$: Capacitor discharging time

$$T_{off} = 0.693 \times 7.5k \times 0.1\mu$$

$$\boxed{T_{off} = 0.525 \text{ msec}}$$

$$T_{total} = T_{ON} + T_{off} = 1.05 + 0.525 = 1.575 \text{ msec}$$

frequency of oscillation $f = \frac{1}{T} = \frac{1}{1.575 \times 10^{-3}} = 635 Hz$



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problem 2.

In problem 1. what should be the value of C for the astable frequency of 300kHz.

Soln:-

$$T = 0.693 (R_1 + R_2) \cdot C$$

$$f = \frac{1.44}{(R_1 + 2R_2) \cdot C} = \frac{1.44}{(3 \times 7.5k) \cdot C} = 300k$$

$$\Rightarrow C = \frac{1.44}{22.5 \times 300 \times 10^6}$$

$$C = 0.213 \times 10^{-9} F$$

(b) $C = 0.213\,\mu F$

dir

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Applications of Astable Multivibrator

➢ ***State the applications of astable multivibrator.***

1. Square wave generator
2. Voltage Controlled Oscillator (VCO)
3. FSK generator
4. Flasher circuit

Problems:

Ex. *A 555 timer configured in astable mode with R_A = 2 kohm, R_B = 4 kohm and C = 0.1 μF. Determine the frequency of the ouptut and duty cycle.*

Sol. :

$$\therefore \quad f = \frac{1.44}{(R_A + 2R_B)C}$$

$$= \frac{1.44}{[2\times 10^3 + 2\times 4\times 10^3]\times 0.1\times 10^{-6}}$$

$$= \mathbf{1.44\ kHz}$$

$$\%\ D = \frac{R_A + R_B}{R_A + 2R_B}$$

$$= \frac{2\times 10^3 + 4\times 10^3}{2\times 10^3 + 2\times 4\times 10^3}\times 100 = \mathbf{60\ \%}$$

Ex. *A 555 timer is configured in a stable mode with R_A = 2 KΩ and R_B = 6 kΩ. Find C if the frequency of the output is 1.028 kHz.*

Sol. : $R_A = 2\ k\Omega, R_B = 6\ k\Omega, f = 1.028\ kHz$

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{i.e.} \quad 1.028\times 10^3 = \frac{1.44}{[2+2\times 6]\times 10^3 \times C}$$

$$\therefore \quad C = \frac{1.44}{1.028\times 10^3 \times 14\times 10^3} = \mathbf{0.1\ \mu F}$$

Question Bank:

MODULE-5

DIGITAL ELECTRONICS FUNDAMENTALS:

Topic 5.1. Difference between and analog and digital signals

Topic 5.2 Number System- Binary, Hexadecimal, Conversion-Decimal to binary, Hexadecimal to decimal and vice-versa, Subtraction using 2's complement method

Topic 5.3 Boolean algebra, Basic and Universal Gates,

Topic 5.4 Combinational circuits:

Half and Full adder,

Multiplexer,

Decoder,

Topic 5.5 Flip Flops : SR and J K Flip flops.

Topic 5.6 Applications of Flip Flops :Shift register, 3 bit ripple Counter

(Text1: 10.1 to 10.7)

Topic 5.7 Basic Communication System, Principle of operations of Mobile Phone (Text 1: 18.2 and 18.8)

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Topic 5.1. Difference between and analog and digital signals

==========

Topic 5.2 Number System- Binary, Hexadecimal, Conversion-Decimal to binary, Hexadecimal to decimal and vice-versa, Subtraction using 2's complement method

1. **Find**
   i. **$(1010111011110101)_2 = (?)_{16}$**
   ii. **$(FA876)_{16} = (?)_2$** **(4 Marks). Dec/Jan 2019**

2. **Perform the following:**
   i. **Convert $(925.75)_{10}$ to base-2 and base-16.**
   ii. **Subtract from $(11011.11)_2$ from $(10101.11)_2$ using 2's complement method. (6Marks) Dec/Jan 2019.**

3. **Subtract the following using 2's complement: (02 marks) Dec/Jan 2019.**
   i. **11100-10011.**

4. **Find**
   i. **$(1101011101101010)_2 = (?)_{16}$**
   ii. **$(EB986)_{16} = (?)_2$**
   iii. **$(925.75)_{10} = (?)_8$ (6 Marks) Dec-Jan 2020.**

5. Convert the following. (8 Marks) MQP-1

i) $(725.25)10=(\ ?\ )_2 = (\ ?\ )_{16}$

ii) $(111100111110001)_2= (\ ?\ )_{10} = (\ ?\ )_{16}$

6. **Perform the following**

(i) Convert $(A\ B\ C\ D)_{16}$ =(?)2=$(?)_8$=(?)10

(ii) Subtract $(1010)_2$-$(111)_2$ using 2's compliment method. (5 Marks) MQP-2

7. Perform the following

(i) Convert $(111110101101)_2$ to $(\ )_8$

(ii) Subtract $(22)_2$-$(17)_2$ using 1's and 2's compliment method. (5 Marks) MQP-2

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Topic 5.3 Boolean algebra, Basic and Universal Gates

1. **State and prove De Morgan's theorems. (4 Marks) Dec/Jan 2019.**
2. **Simplify** $S = A \oplus B \oplus C$ **and realize using basic gates. (05 marks) Dec/Jan 2019.**
3. **Simplify the following expressions and draw the logic circuits using basic gates.**
   i) AB+ A'C+ AB' C (AB+C)
   ii) (A+B')(CD+E) (6 Marks) MQP-1
4. **Realize Y=AB+CD+E using NAND gates. (4 Marks) MQP-2**
5. **Simplify and realize the following using NAND gates only**
   i) Y=AC+ ABC+A' BC+ AB+D
   ii) Y=A B´C'+A'B´C'+A'B'+A'C' (6 Marks) MQP-3

6. **Simplify the following Boolean expressions**
   (i) Y=A B' + AB
   (ii) Y=AB+ AC+BD+CD
   (iii) Y=(B+CA)(C+A' B)
   (iv) Y=A´B´C´D'+A´B´C'D+ A B´C´D'+ AB´C'D (8 Marks) MQP-3

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Topic 5.4 Combinational circuits: Half and Full adder, Multiplexer, Decoder.

1. **Design Full adder circuit and implement it using basic gates. (10Marks). Dec/Jan 2019/ (08 Marks) Dec-Jan 2020.**
2. **Realize/Implment full adder using two half adders. (04 Marks) Dec/Jan 2019./ (6 Marks) MQP-1**
3. **Design full adder circuit using three variables and implement it using two half adders. (8 Marks) MQP-2**

4. **With a neat circuit diagram and truth table, explain the full adder circuit. (6 Marks) MQP-3**

5. **What is multiplexer? Implement 8:1 multiplexer using basic gates. (08 Marks) Dec/Jan 2019.**

6. **What is a multiplexer? Explain the working of 4:1 multiplexer. (6 Marks) MQP-1**

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Topic 5.5 Flip Flops : SR and J K Flip flops.

1. **Explain the working of RS flip flop with truth table and diagram. (06 Marks) Dec/Jan 2019.**

2. **With the help of a logic diagram and truth table, explain the working of a clocked SR flip-flop. (6 Marks) MQP-1**

3. **What is Flip Flop ? Explain the operation of master slave JK flip Flop. (08 marks) Dec/Jan 2019./MQP2**

4. **With a neat circuit diagram and truth table, explain the working of a JK flip flop. (6 Marks) MQP-3**

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Topic 5.6 Applications of Flip Flops :Shift register, 3 bit ripple Counter

1. **Explain the working of a 3-bit ripple counter with neat circuit diagram and timing diagrams. (8Marks) Dec/Jan 2019.**

2. **What is a counter? With a neat timing and block diagram, explain three bit asynchronous counter operation. (7 Marks) MQP-2**

3. **What is a shift register? Explain the working of a 4-bit SISO shift register. (8 Marks) MQP-1**

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Topic 5.7 Basic Communication System, Principle of operations of Mobile Phone

1. **Explain the basic elements of communication system with block diagram. (6 Marks). Dec/Jan 2019.**

2. **With a neat block diagram, explain the operating principle of the GSM system. (6 Marks) MQP-2/MQP3**

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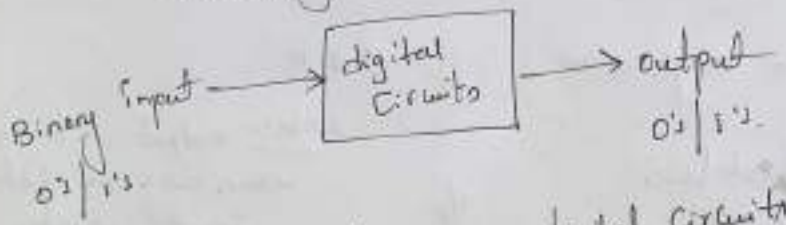
Logic Gates :-

* Building blocks of Digital System.



Defn :- There are basically digital circuits that are designed to 'Execute' Logical functions like 'Boolean addition', 'Boolean multiplication' and inversion etc.

Classification :-

We use algebraic Expressions in order to show the operation performed by the logic gates.

i. OR Gate

Logic Symbol

2 i/p OR gate

Boolean expression $y = a + b$.

Note:- output is high when any one of the input is high.

Truth table:-

i/p a	i/p b	o/p Y = a+b
0	0	0
0	1	1
1	0	1
1	0	1

2 distinct i/ps = $2^2 = 4$ combinations

Important Boolean identities related to OR Gate:-

a	b	o/p Y = a+b
i. 0	0	x → x
ii. 0	1	1
iii. 1	0	1
iv. 1	1	1

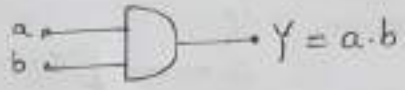
i) ii) iii) iv)

xi.
i. $0 + x = x$
ii. $1 + x = 1$
iii. $x + \bar{x} = 1$
iv. $x + x = x$

ii. AND Gate :-

2 i/p AND Gate

Symbol :-



Logical expression : $Y = a \cdot b$

Note :- The output is high only when all inputs are high.

Truth table :

i/p a	i/p b	o/p Y = a·b
0	0	0
0	1	0
1	0	0
1	1	1

Important Boolean identities related to AND Logic :-

i/p a	i/p b	o/p Y = a·b
0	0	0
0	1	0
1	0	0
1	1	1

i. $0 \cdot x = 0$
ii. $1 \cdot x = x$
iii. $x \cdot \bar{x} = 0$
iv. $x \cdot x = x$

iii) NOT Gate

Symbol:

Logical expression : $y = \bar{a}$

truth table :-

a i/p	Y o/p
0	1
1	0

Note:- The output is complement of the input.

iv) NAND Gate :- AND followed by NOT

Symbol :-

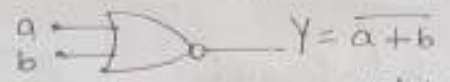
Logical Expression :- $y = \overline{ab}$

Truth table :-

a i/p	b i/p	$y = \overline{ab}$ o/p
0	0	1
0	1	1
1	0	1
1	1	0

Note:- The output is high only when one of the input is Low.

v. NOR Gate:- OR followed by NOT

Symbol 

Note:- The output is high when all the inputs are low.

Logical Expression :- $Y = \overline{a+b}$

Truth table:-

a	b	$Y = \overline{a+b}$
0	0	1
0	1	0
1	0	0
1	1	0

vi Ex-OR gate:-

Symbol :- 

Logical expression :- $Y = a \oplus b = \bar{a}b + a\bar{b}$

Truth table:-

i/p a	i/p b	o/p $Y = a \oplus b$
0	0	0
0	1	1
1	0	1
1	1	0

Note:- The output is high when odd number of inputs are high.

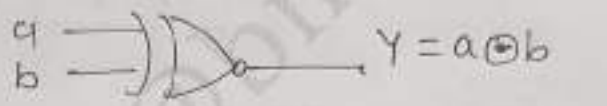
Boolean identities related to Ex-OR logic

a	b	$Y = a \oplus b$
0	0	0
0	1	1
1	0	1
1	1	0

i. $0 \oplus x = x$
ii. $1 \oplus x = \bar{x}$
iii. $x \oplus \bar{x} = 1$
iv. $x \oplus x = 0$

vii Ex-NOR Logic Gate: [Ex-OR followed by NOT]

Symbol



Logic Expression: $Y = a \odot b = ab + \bar{a}\bar{b} = \overline{a \oplus b}$

Truth table:

a	b	$Y = a \odot b$
0	0	1
0	1	0
1	0	0
1	1	1

Note: The output is high only when Even number of ones at the input.

Boolean identities related to Ex-NOR logic:

a	b	$Y = a \odot b$
0	0	1
0	1	0
1	0	0
1	1	1

i. $0 \odot x = \bar{x}$
ii. $1 \odot x = x$
iii. $x \odot \bar{x} = 0$
iv. $x \odot x = 1$

Laws of Boolean Algebra:-

1. Commutative Laws

✓ $a+b = b+a$

proof:

a	b	a+b
0	0	0
0	1	1
1	0	1
1	1	1

$\Leftrightarrow$

a	b	b+a
0	0	0
0	1	1
1	0	1
1	1	1

✓

ii. $a \cdot b = b \cdot a$

proof:

a	b	a·b
0	0	0
0	1	0
1	0	0
1	1	1

$\Leftrightarrow$

a	b	b·a
0	0	0
0	1	0
1	0	0
1	1	1

Note:- Ily for 3 variable.

i. $a+b+c = c+b+a$

ii. $abc = cba$

ii. Associative laws:

i. $a+(b+c) = (a+b)+c$

ii. $(ab)c = a(bc)$.

proof: i. $a+(b+c) = (a+b)+c$

a	b	c	(b+c)	a+(b+c) (LHS)	(a+b)	(a+b)+c (RHS)
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

Obs:- LHS = RHS.

ii. $(ab)c = a(bc)$

By construct a truth table

LHS Equal RHS

a	b	c	ab	(ab)c	(bc)	a(bc)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

obs: LHS = RHS.

iii) Distributive Law: $a(b+c) = ab + ac$

Proof:

a	b	c	(b+c)	a(b+c) (LHS)	ab	ac (Equal)	ab+ac (RHS)
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

Boolean identities :-

used to simplify Boolean functions

i. $0 + a = a$

ii. $1 + a = 1$

iii. $a + a = a$

iv. $a + \bar{a} = 1$

v. $a \cdot 0 = 0$

vi. $1 \cdot a = a$

vii. $a \cdot a = a$

ix. $a \cdot \bar{a} = 0$

x. $\bar{\bar{a}} = a$

xi. $a + ab = a$

proof: $a + ab = a(1 + b)$

1 (rule ii)

$= a \cdot 1$

$= a$

xii. $a + \bar{a}b = a + b$

proof: LHS $a + \bar{a}b$

using rule xi: $a + ab = a$

$= a + ab + \bar{a}b$

$= a + b(a + \bar{a})$

using rule (iv) $a + \bar{a} = 1$

$= a + b \cdot (1)$

$= a + b$ (RHS)

xiii. $(a+b)(a+c) = a + bc$

proof:- LHS

$= (a+b)(a+c)$

using distributive law

$= aa + ac + ba + bc$

using rule (vii) $a \cdot a = a$

$= a + ac + ba + bc$

$= a(1 + c) + ba + bc$

$= a + ba + bc = a(1 + b) + bc$

$= a \cdot 1 + bc = a + bc = RHS$

Q. State the identities of Boolean addition and Boolean Multiplication.

Soln:

i. Identities of Boolean addition

$$a+0=a$$
$$a+1=1$$
$$a+a=a$$
$$a+\bar{a}=1$$

ii. Identities of Boolean Multiplication

$$a\cdot 0=0$$
$$a\cdot 1=a$$
$$a\cdot a=a$$
$$a\cdot \bar{a}=0$$

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5d.

Topic 5.3 Boolean algebra, Basic and Universal Gates

State and prove De Morgan's theorems. **(4 Marks) Dec/Jan 2019.**

Soln:- De Morgan's Suggested two theorems that form an important part of Boolean algebra.

i.e. $\overline{ab} = \overline{a} + \overline{b}$

i.e Complement of a product is equal to the Sum of the complements.

Proof:

LHS = $\overline{ab}$, RHS = $\overline{a} + \overline{b}$, Equal

a	b	ab	$\overline{ab}$	$\overline{a}$	$\overline{b}$	$\overline{a} + \overline{b}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

i.e. $\overline{a+b} = \overline{a} \cdot \overline{b}$

i.e The Complement of a Sum is equal to the product of the complements.

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proof.

L.H.S equal R.H.S

a	b	a+b	$\overline{a+b}$	$\bar{a}$	$\bar{b}$	$\bar{a}\cdot\bar{b}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

i. Note: Demorgan's theorem for 3 variables

$$\overline{abc} = \bar{a} + \bar{b} + \bar{c}$$

$$\overline{a+b+c} = \bar{a}\cdot\bar{b}\cdot\bar{c}$$

Note2. My for 4-variables

$$\overline{abcd} = \bar{a} + \bar{b} + \bar{c} + \bar{d}$$

$$\overline{a+b+c+d} = \bar{a}\cdot\bar{b}\cdot\bar{c}\cdot\bar{d}$$

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Simplify $S = A \oplus B \oplus C$ and realize using basic gates. **(05 marks) Dec/Jan 2019.**

$S = A \oplus B \oplus C$

given boolean expression in a three-input Ex-OR logic

w.k.t $a \oplus b = a\bar{b} + \bar{a}b$

let $x = a \oplus b$; $\bar{x} = \overline{a \oplus b} = a \odot b = \bar{a}\bar{b} + ab$

$S = x \oplus C = x\bar{C} + \bar{x}C$

$= [a\bar{b} + \bar{a}b]\bar{C} + [\bar{a}\bar{b} + ab]C$

$= a\bar{b}\bar{C} + \bar{a}b\bar{C} + \bar{a}\bar{b}C + abC$

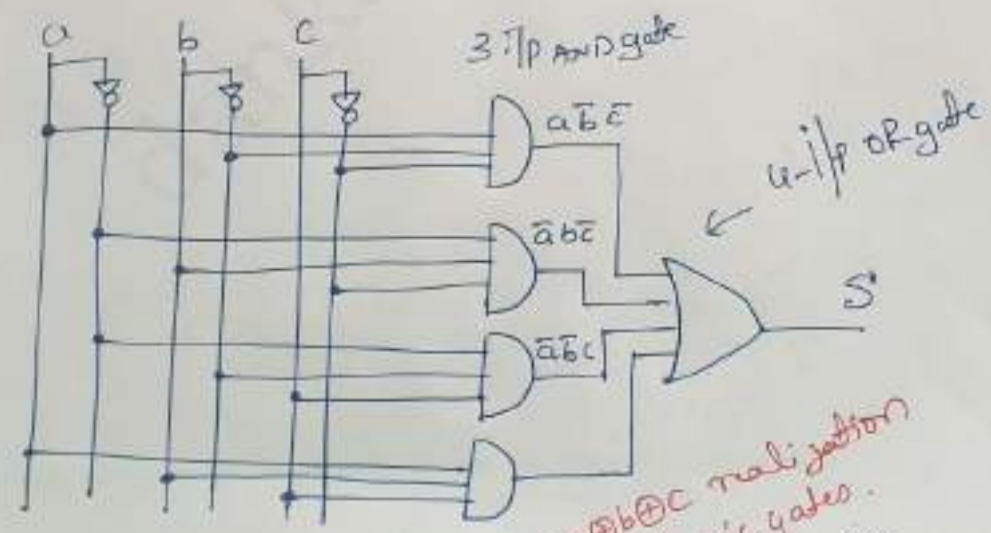

fig: $S = a \oplus b \oplus c$ realization using basic gates.

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Simplify the following expressions and draw the logic circuits using basic gates.

i) AB+ A'C+ AB' C (AB+C)

ii) (A+B')(CD+E)

(6 Marks) MQP-1

Soln'r

$$Y = AB + \bar{A}C + A\bar{B}C(AB + C)$$

using distributive law

$$= AB + \bar{A}C + A\bar{B}CAB + A\bar{B}CC$$

using commutative law

$$= AB + \bar{A}C + AA\bar{B}\bar{B}C + A\bar{B}CC$$

$B\bar{B} = 0$ and $CC = C$

using identity

$$= AB + \bar{A}C + A\bar{B}C$$

$$= AB + (\bar{A} + A\bar{B})C$$

$$= AB + [(\bar{A} + A)\cdot(\bar{A} + \bar{B})]C$$

$$= AB + (\bar{A} + \bar{B})C$$

$$= AB + \bar{A}C + \bar{B}C$$

$$= AB + [\bar{A} + \bar{B}]C$$

$$= AB + (\bar{A}\bar{B})\cdot C$$

$$\boxed{Y = AB + C}$$

$\bar{A} + A\bar{B} = (\bar{A} + A)(\bar{A} + \bar{B})$

$= \bar{A}\cdot\bar{A} + \bar{A}\bar{B} + A\cdot\bar{A} + A\bar{B}$

$= \bar{A} + \bar{A}\bar{B} + 0 + A\bar{B}$

$= \bar{A}(1 + \bar{B}) + A\bar{B}$

$= \bar{A}(1) + A\bar{B}$

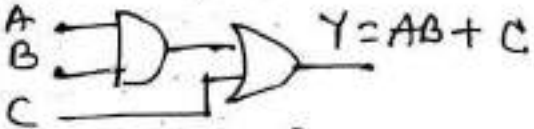
$= \bar{A} + A\bar{B}$

Say $AB = x$

$= x + \bar{x}C$

$= (x + \bar{x})(x + C)$

$= (x + C)$



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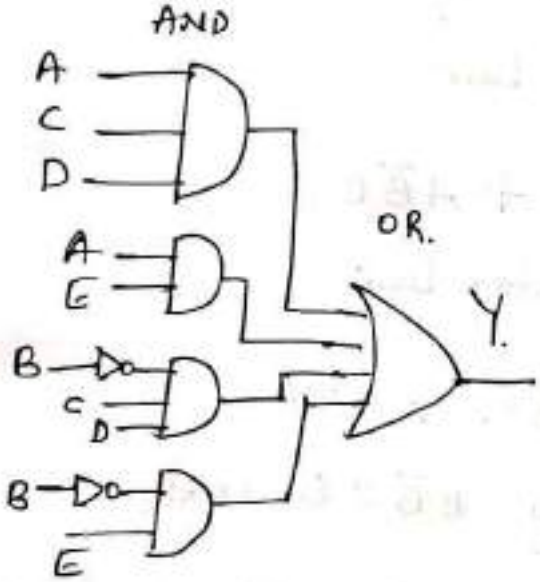
ii) $Y = (A+\bar{B})(CD+E)$

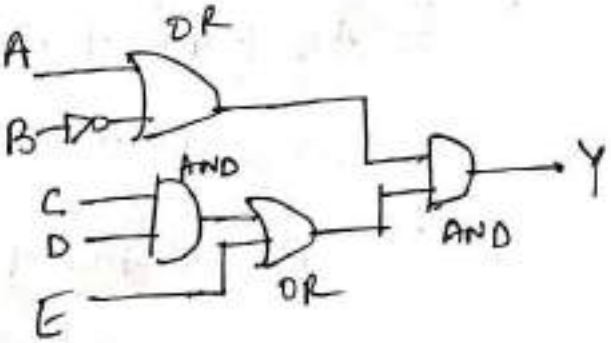
using distributive Law

$$\boxed{Y = ACD + AE + \bar{B}CD + \bar{B}E}$$



$Y = (A+\bar{B})(CD+E)$

(a)



3. Show that $a + bc = (a+b)(a+c)$

Soln: R.H.S $= (a+b)(a+c)$

using distributive law

$= aa + ac + ba + bc$

$a \cdot a = a$

$= a + a(b+c) + bc$

$= a[1 + (b+c)] + bc$

$= a + bc$ (LHS)

Say $b+c = x$

$1 + (b+c) = 1 + x$

$= 1$

W.K.T $1 + a = 1$

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Simplify the following Boolean expressions

(i) Y=A B' + AB
(ii) Y=AB+ AC+BD+CD
(iii) Y=(B+CA)(C+A' B)
(iv) Y=A'B'C'D'+A'B'C'D+ A B'C'D'+ AB'C'D

(8 Marks) MQP-3

Soln: i. $Y = A\bar{B} + AB$

$= A(\bar{B} + B)$ | $B + \bar{B} = 1$

$= A \cdot (1)$

$\boxed{Y = A}$

ii. $Y = AB + AC + BD + CD$

$Y = AB + BD + AC + CD$

$Y = B(A+D) + C(A+D)$

$\boxed{Y = (A+D)(B+C)}$

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iii) $Y = (B + CA)(C + \bar{A}B)$

using distributive Law

$= BC + \bar{A}BB + CCA + CA\bar{A}B$

$CA\bar{A}B \rightarrow 0$

$\boxed{Y = BC + \bar{A}B + CA}$

using Boolean identities
$BB = B$
$CC = C$
$A \cdot \bar{A} = 0$

iv) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$

$= \bar{A}\bar{B}\bar{C}[\bar{D} + D] + A\bar{B}\bar{C}[\bar{D} + D]$

$\bar{D} + D \rightarrow 1$ using Boolean identity $0 + \bar{D} = 1$.

$= \bar{A}\bar{B}\bar{C} \cdot (1) + A\bar{B}\bar{C} \cdot (1)$

$= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$

$= \bar{B}\bar{C}(\bar{A} + A)$

$\boxed{Y = \bar{B}\bar{C}}$

$A + \bar{A} = 1$

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Simplification of Boolean Expressions

e. prove that $\overline{\overline{AB} + \bar{A} + AB} = 0$

Soln:- L.H.S

$$= \overline{\overline{AB} + \bar{A} + AB}$$

let $AB = x$

and $\overline{AB} = \bar{x}$

$$\therefore = \overline{\bar{x} + \bar{A} + x} \quad \text{: using Commutative Law}$$

$$= \overline{(x + \bar{x}) + \bar{A}}$$

$x + \bar{x} = 1$

$$= \overline{(1 + \bar{A})}$$

$1 + \bar{A} = 1$

$$= \overline{(1)}$$

$$= 0$$

ii. Simplify $ABC + AB\bar{C} + \bar{A}BC$

$$Y = ABC + AB\bar{C} + \bar{A}BC$$

$$= AB(C + \bar{C}) + \bar{A}BC$$

$C + \bar{C} = 1$

$$= AB + \bar{A}BC$$

$A + \bar{A}C = A + C$

$$= B(A + \bar{A}C)$$

$$= B(A + C)$$

$= (A + \bar{A})(A + C)$

$= 1 \cdot (A + C)$

$$= AB + BC$$

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iii) $AB + \overline{A}\overline{C} + A\overline{B}C(AB+C)$

using demorgan's law & distributive laws

$= AB + (\overline{A} + \overline{C}) + A\overline{B}C.AB + A\overline{B}CC$

$= AB + \overline{A} + \overline{C} + AA\overline{B}.\overline{B}C + A\overline{B}CC$

$B.\overline{B} = 0$ & $CC = 1$.

$= AB + \overline{A} + \overline{C} + A\overline{B}C$ | using $w + xy = (w+x)(w+y)$

$= (\overline{A} + BA) + (\overline{C} + CA\overline{B})$

$= (\overline{A} + B)(A + \overline{A}) + (C + \overline{C}).(\overline{C} + A\overline{B})$

$(A + \overline{A}) = 1$, $(C + \overline{C}) = 1$

$= \overline{A} + B + \overline{C} + A\overline{B}$

$= \overline{A} + \overline{C} + (B + A\overline{B})$

$= \overline{A} + \overline{C} + (B+A)(B+\overline{B})$

$(B + \overline{B}) = 1$

$= \overline{A} + \overline{C} + B + A$

$= (A + \overline{A}) + B + \overline{C}$

$(A + \overline{A}) = 1$

$= 1 + (B + \overline{C})$ — say x

$= 1 + x$

$= 1$

$1 + x = 1$

(A) $= (1 + B) + \overline{C}$

$= 1 + \overline{C}$

$= 1$ ✓

iv) $\overline{A\bar{B} + ABC + A(B+A\bar{B})}$

Soln:-

$= \overline{\overline{A(\bar{B}+BC)} + A(B+A)}$; using $B+A\bar{B} = (B+A)(B+\bar{B}) = (B+A)$

$\bar{B}+BC = (\bar{B}+B)(\bar{B}+C)$

$= (\bar{B}+C)$

$= \overline{\overline{A\cdot(\bar{B}+C)} + A(B+A)}$

using demorgan's law & distributive law

$\overline{A\cdot(\bar{B}+C)} = \bar{A} + \overline{(\bar{B}+C)}$

$= \overline{\bar{A} + \overline{(\bar{B}+C)} + AB + AA}$

using Demorgan's law $\overline{\bar{B}+C} = \bar{\bar{B}}\cdot\bar{C} = B\bar{C}$ & $AA = A$

$= \overline{\bar{A} + B\bar{C} + AB + A}$

$= \overline{(A+\bar{A}) + B\bar{C} + AB}$

$A+\bar{A} = 1$

$= \overline{1 + (B\bar{C} + AB)}$

$1 + x = 1$

$= \overline{1} = 0$

Implementation of Boolean functions

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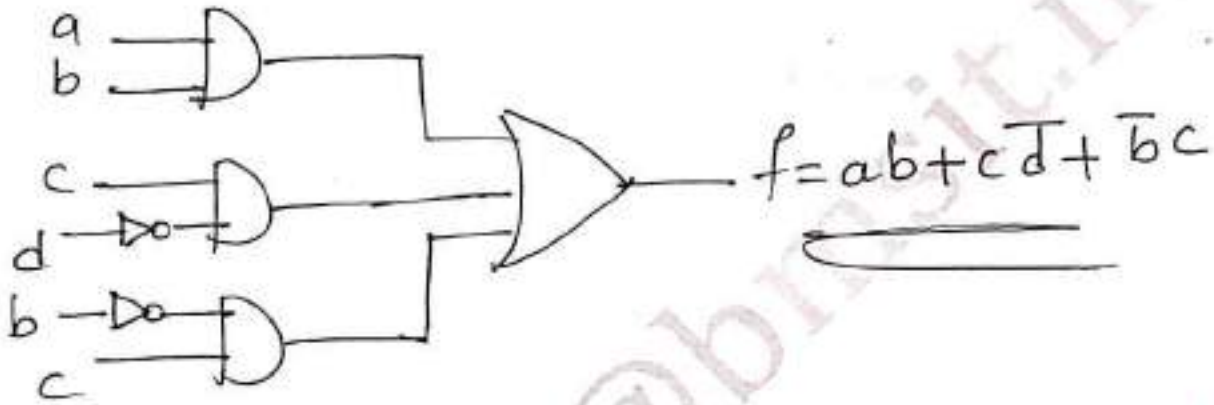
Q1) $f = ab + c\bar{d} + \bar{b}c$

3 product terms



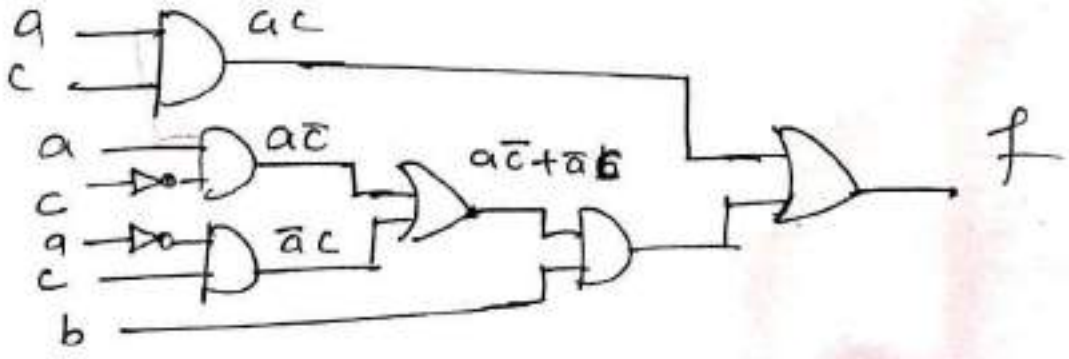
Q2. Simplify $abc + a\bar{b}c + ab\bar{c} + \bar{a}bc$ and realize using basic gates.

Soln:- $f = \underset{111}{abc} + \underset{101}{a\bar{b}c} + \underset{110}{ab\bar{c}} + \underset{011}{\bar{a}bc}$

$f = ac(b + \bar{b}) + b(a\bar{c} + \bar{a}c)$

$b + \bar{b} = 1$

$$\boxed{f = ac + b(a\bar{c} + \bar{a}c)}$$



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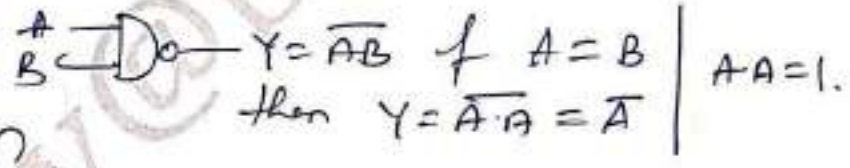
Universal Gates:-

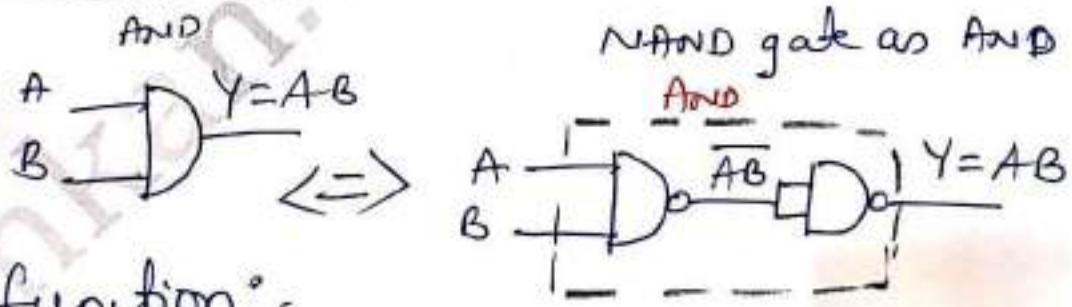
The NAND and NOR gates are known as Universal gates, since any Logic function can be implemented using NAND (or) NOR gates alone.

Case i:- NAND as Universal gate

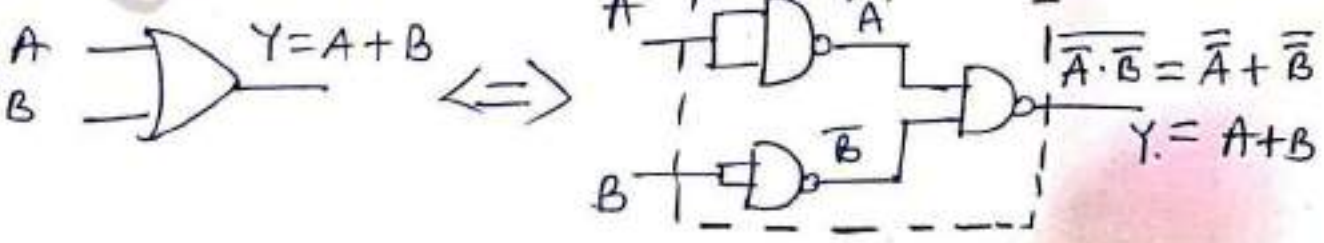
i. NOT function.



ii. AND function



iii. OR function:-



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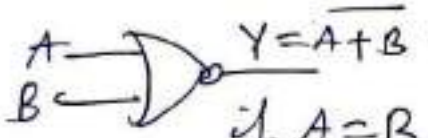
ii. NOR as Universal

→ AND, NOT, OR

i. NOT gate

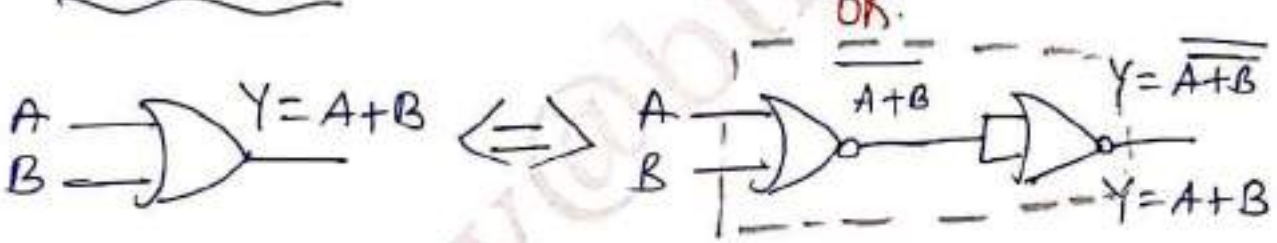
i.e 

if A=B

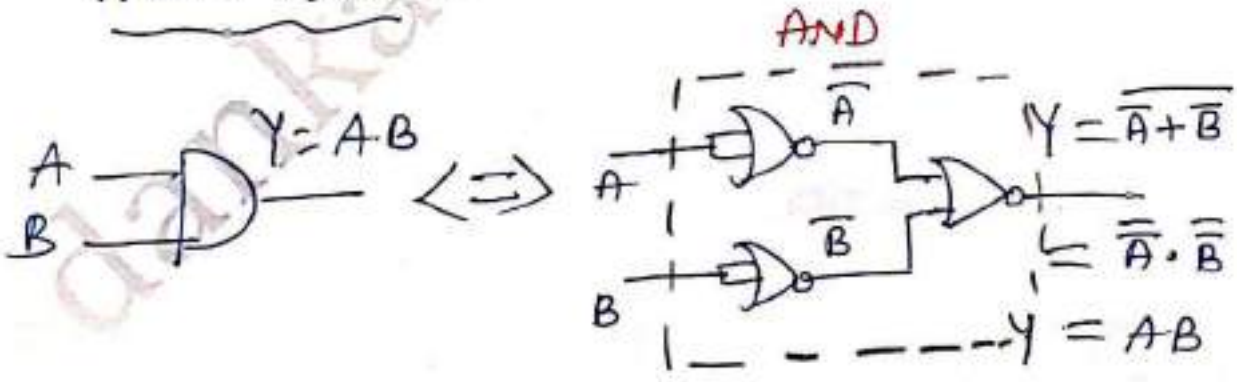
$Y = A + A = \bar{A}$

but $(A+A) = A$

ii. OR Gate :-



iii. AND Gate :-



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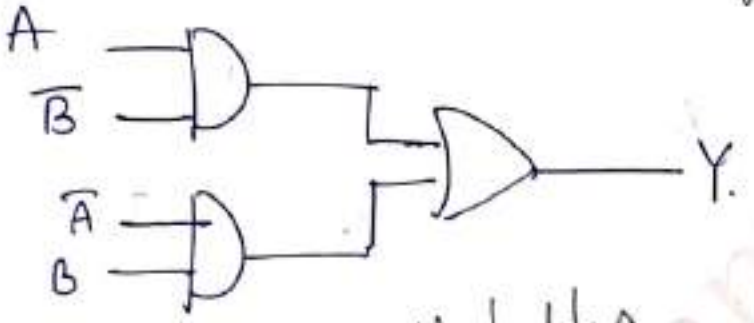
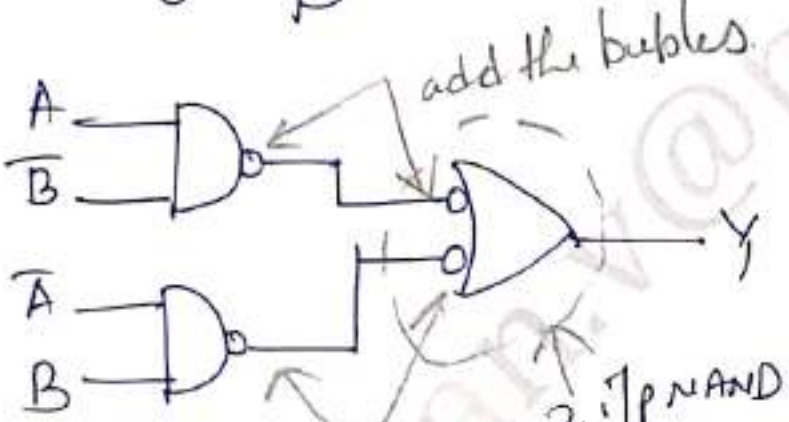
8. Implement Ex-OR gate using only NAND gates.

Soln:- Ex-OR Logic $Y = A \oplus B$

$Y = A\bar{B} + \bar{A}B$.

sum of product term.





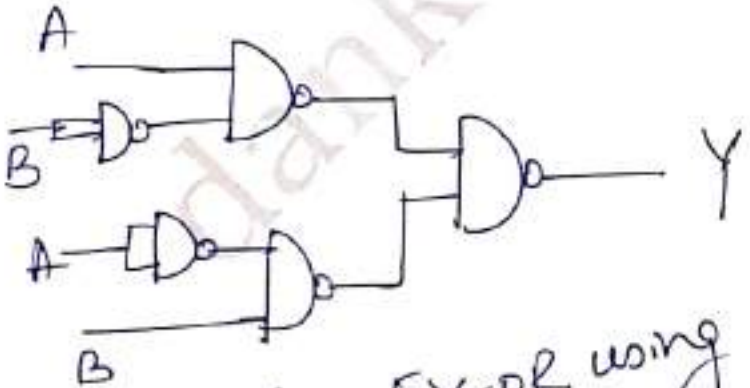
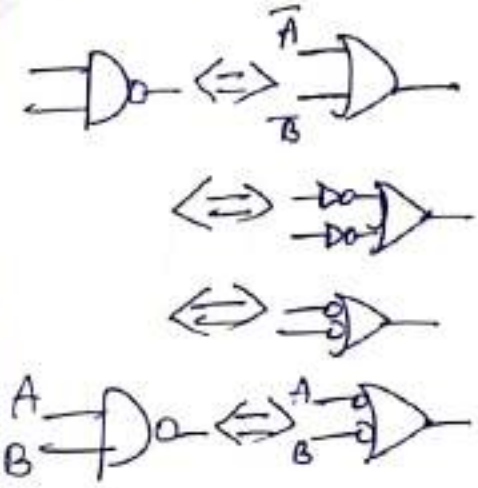


fig:- EX-OR using NAND alone.

Note:-

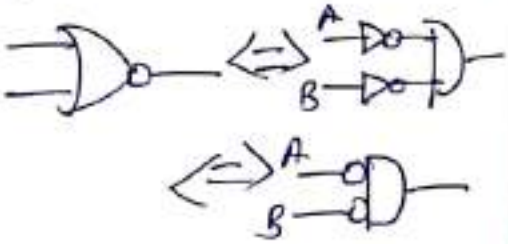
Demorgan's law

i: $\overline{AB} = \bar{A} + \bar{B}$

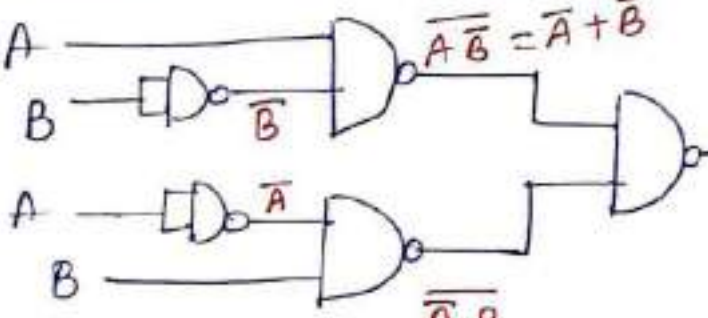


and

ii: $\overline{A+B} = \bar{A} \cdot \bar{B}$



Verification :-



$\overline{A}\,\overline{B} = \overline{A} + \overline{\overline{B}}$

$= \overline{A} + B$

$\overline{A \cdot B}$

$= \overline{A} + \overline{B}$

$= \overline{\overline{A}} + \overline{B}$

$Y = \overline{(\overline{A}+B)\cdot(A+\overline{B})}$

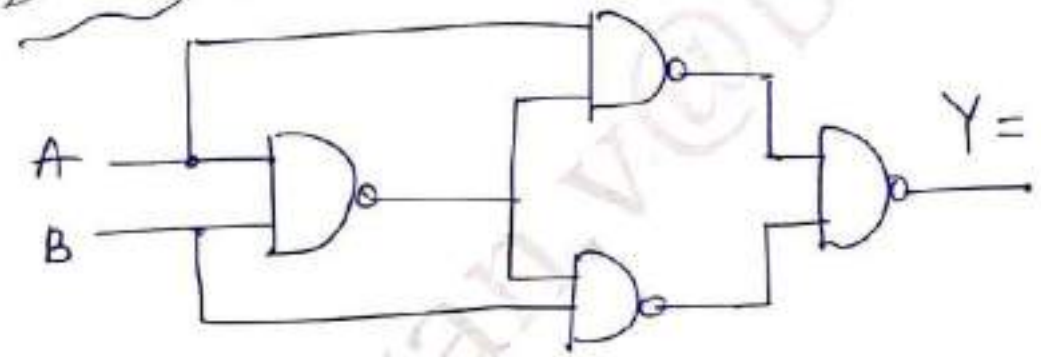
$= \overline{\overline{A}+B} + \overline{A+\overline{B}}$

$= \overline{\overline{A}} \cdot \overline{B} + \overline{A} \cdot \overline{\overline{B}}$

$= A \cdot \overline{B} + \overline{A} \cdot B$

$= A \oplus B$ (Ex-OR logic).

2nd Method



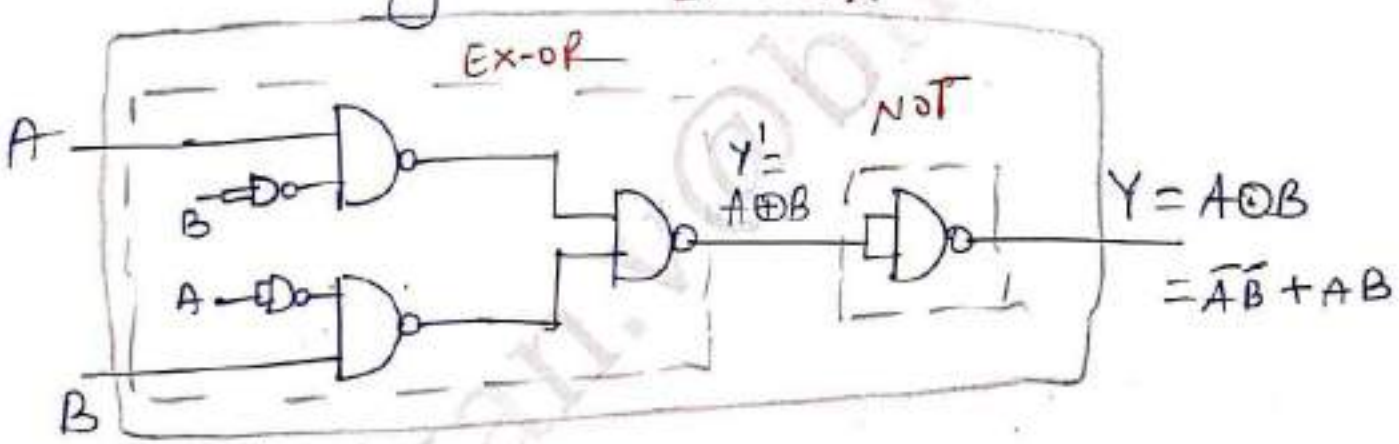
8. Implement Ex-NOR gate using only NAND gates.

Soln:- W.K.T Ex-OR and Ex-NOR are complement to each other.

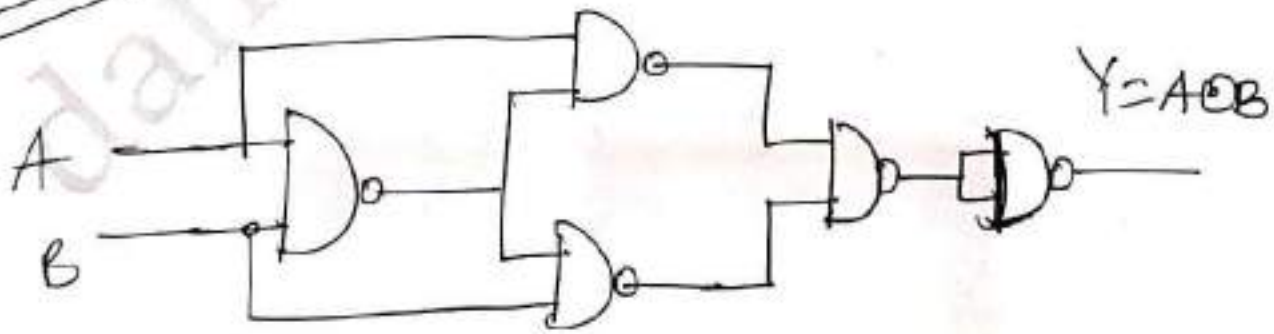
i.e $f = \overline{a \oplus b} = a \odot b$.

i.e Invert the Ex-OR output to get Ex-NOR

Logic.



2nd Method



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8. Implement Ex-NOR using NOR gate. → Make it (OR-AND Logic)

Soln:- Ex-NOR Logic

$$Y = a \odot b = \bar{a}\bar{b} + ab$$

(or)

$$Y = a \odot b = \overline{a \oplus b}$$

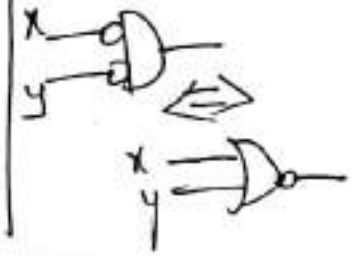
$$Y = \overline{a\bar{b} + \bar{a}b}$$ using Demorgan's law

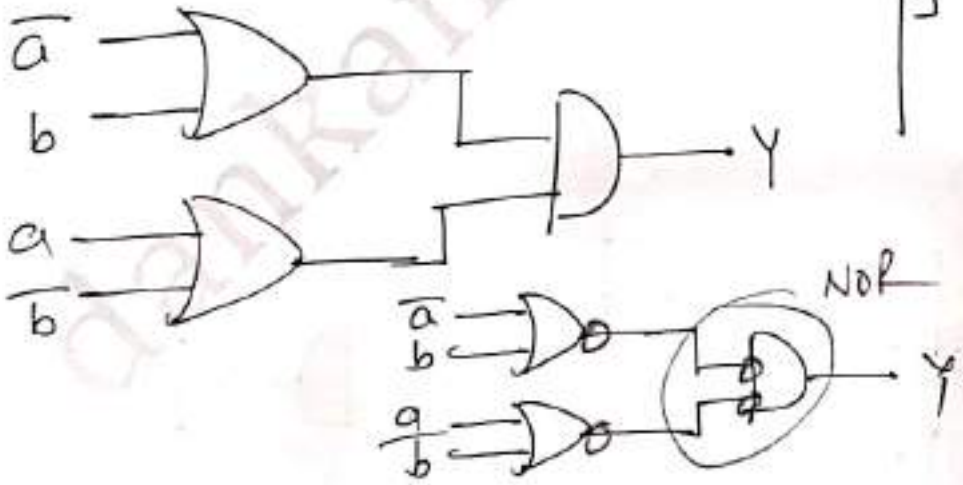
$$= \overline{a\bar{b}} \cdot \overline{\bar{a}b}$$

$$= (\bar{a} + \bar{\bar{b}}) \cdot (\bar{\bar{a}} + \bar{b})$$

$$Y = (\bar{a} + b) \cdot (a + \bar{b})$$

Note:-





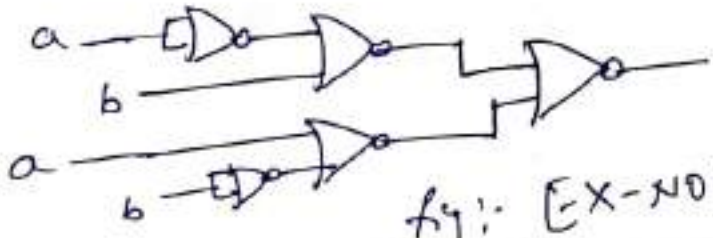
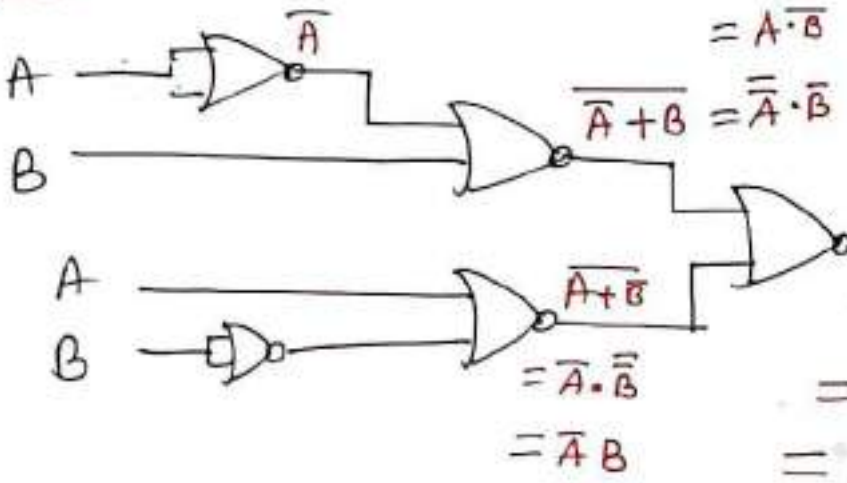


fig:- Ex-NOR using NOR alone.

Verification :-



$= A \cdot \overline{B}$

$\overline{A+B} = \overline{A} \cdot \overline{B}$

$= \overline{A} \cdot \overline{\overline{B}}$

$= \overline{A}B$

$= \overline{A\overline{B}} \cdot \overline{\overline{A}B}$

$= (\overline{A}+\overline{\overline{B}}) \cdot (\overline{\overline{A}}+\overline{B})$

$= (\overline{A}+B)(A+\overline{B})$

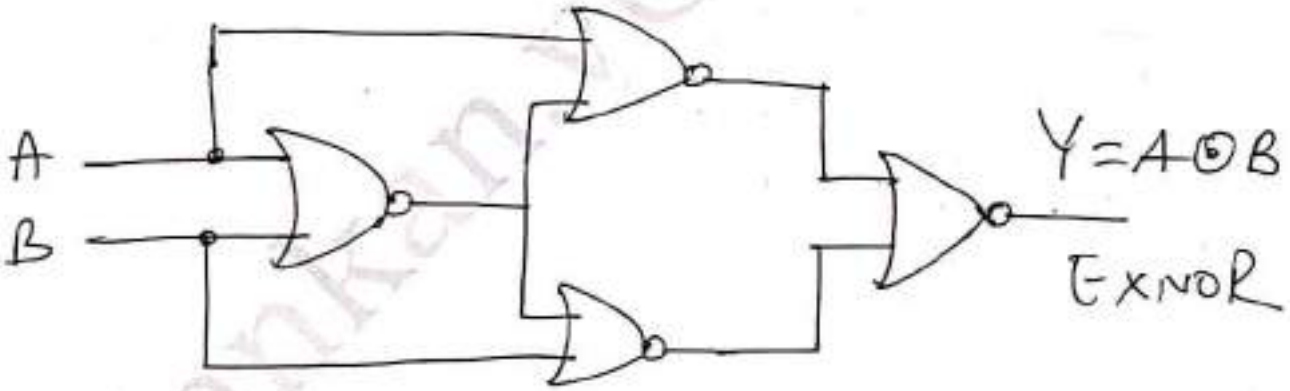
$= \overline{A}A + \overline{A}\,\overline{B} + AB + B\overline{B}$

$= 0 \quad\quad 0$

$= \overline{A}\,\overline{B} + AB = A \odot B$

Ex-NOR logic

2nd Method



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8. Implement the following boolean function with NAND-NAND logic.

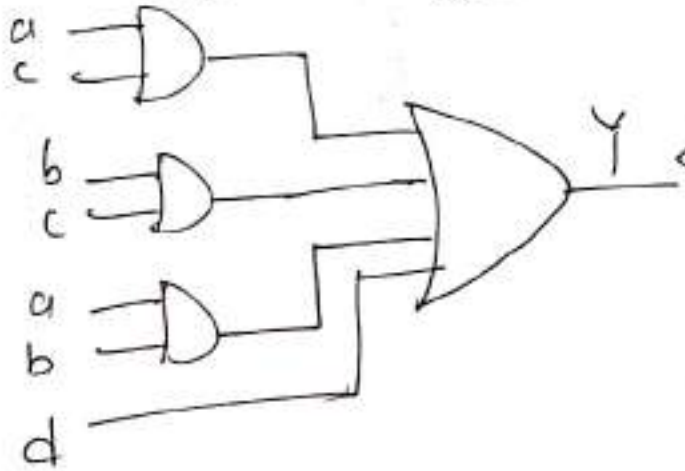
S i) $Y = ac + abc + \bar{a}bc + ab + d$

Soln:- Step1. Simplify the given boolean fn (if possible)

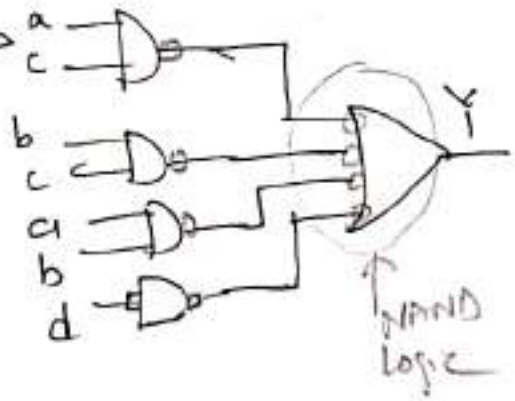
$Y = ac + bc(a + \bar{a}) + ab + d$

$Y = ac + bc + ab + d$ ← AND-OR logic

Step2 Implement using AND-OR logic



Step3. Convert AND-OR logic to NAND-NAND logic



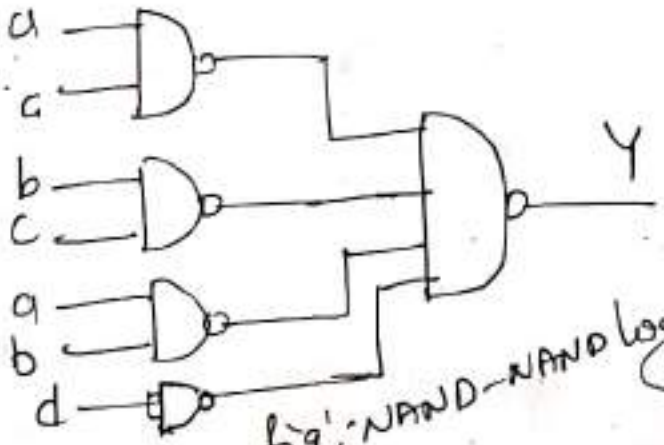


fig: NAND-NAND logic.

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Simplify and realize the following using NAND gates only
i) Y=AC+ ABC+A' BC+ AB+D → previous page
ii) Y=A B'C'+A'B'C'+A'B'+A'C' **(6 Marks)** **MQP-3**

Soln:- ii) $Y = a\bar{b}\bar{c} + \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c}$

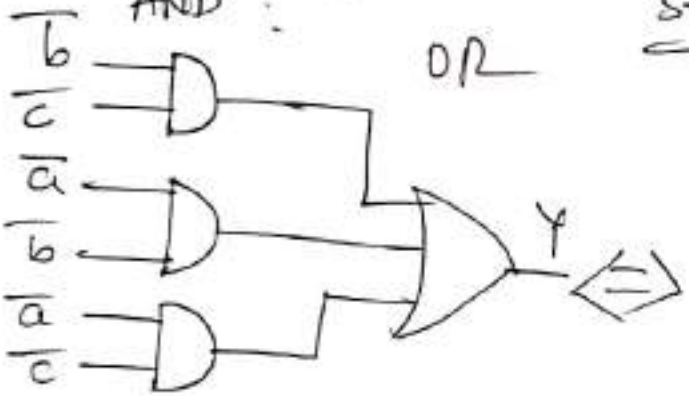
Step1. Simplify the given boolean expression (if possible)

$Y = (a+\bar{a})\bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c}$

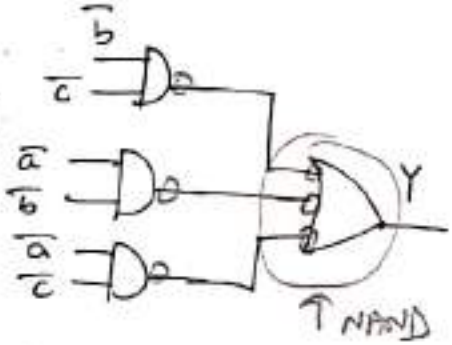
$(a+\bar{a}) = 1$

$$\boxed{Y = \bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c}}$$ ← AND-OR logic.

Step2.



Step-3 NAND-NAND logic



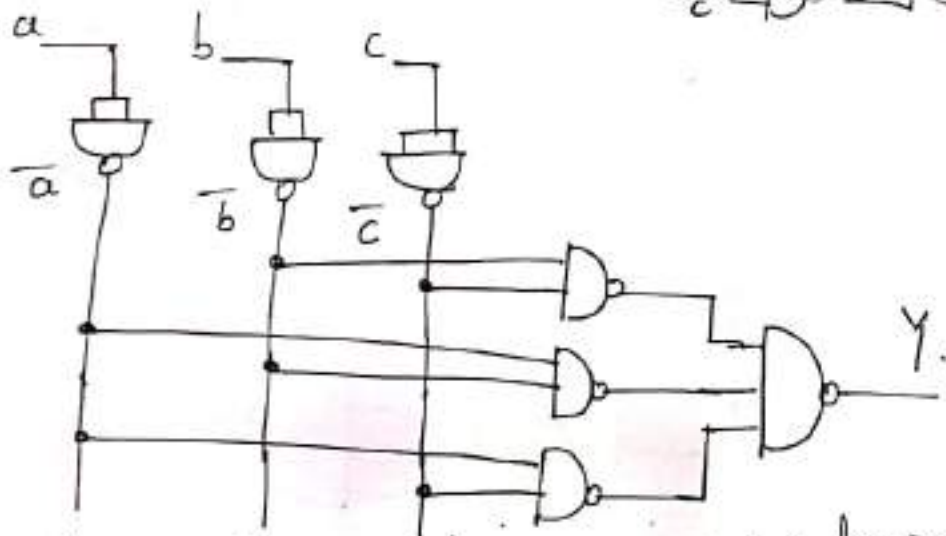


fig:- implementation using NAND gates only.

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NOR - NOR Implementation

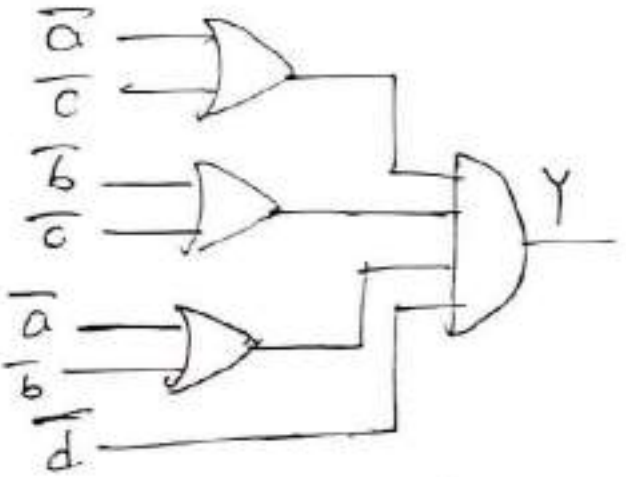
Q. $Y = ac + bc + ab + d$ Realize using only NOR gates.

Soln:- **Step1.** express given Boolean fn into POS form. (product of Sum).

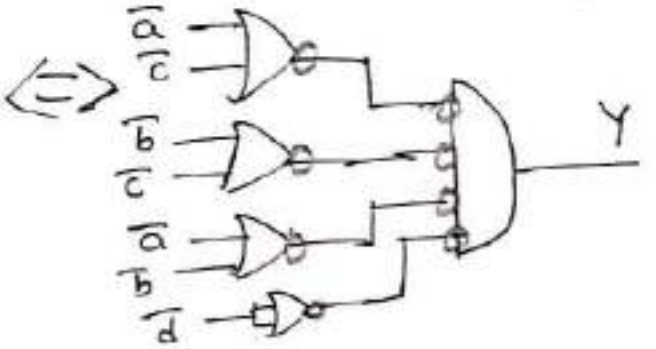
$$\overline{Y} = \overline{ac + bc + ab + d} = \overline{ac} \cdot \overline{bc} \cdot \overline{ab} \cdot \overline{d}$$

$$\overline{Y} = (\bar{a}+\bar{c}) \cdot (\bar{b}+\bar{c}) \cdot (\bar{a}+\bar{b}) \cdot \bar{d}$$

Step2. Implement using OR-AND logic.



Step3. Convert OR-AND logic to NOR-NOR logic



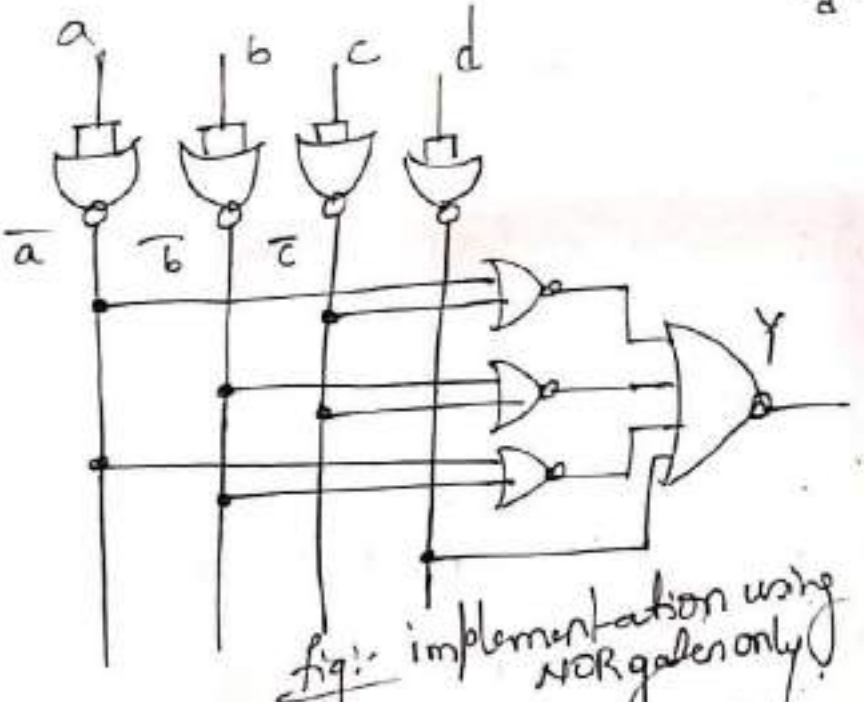


fig:- implementation using NOR gates only

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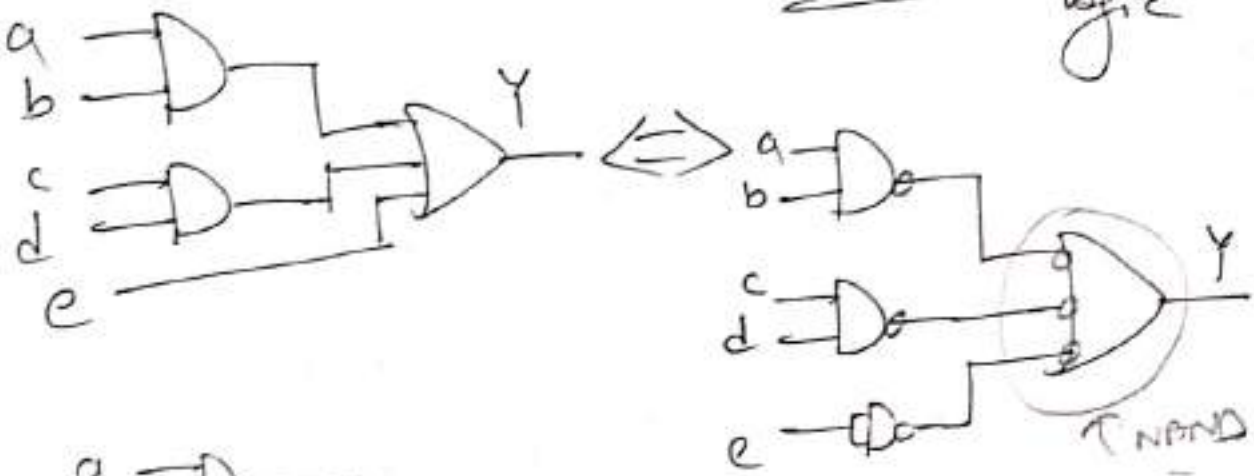
Q:- Realize Y=AB+CD+E using NAND gates. (4 Marks) MQP-2

Soln:- $Y = AB + CD + E$

Step1. further simplification (not-possible)

Step2:- AND-OR logic

Step3. NAND-NAND logic



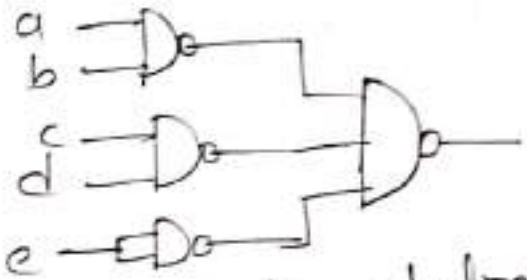


fig:- implementation using NAND alone.

Q. Realize $f = (\bar{a}+b)c$ using NOR-NOR logic.

soln:- given exp. is already in POS form.
implement using OR-AND logic

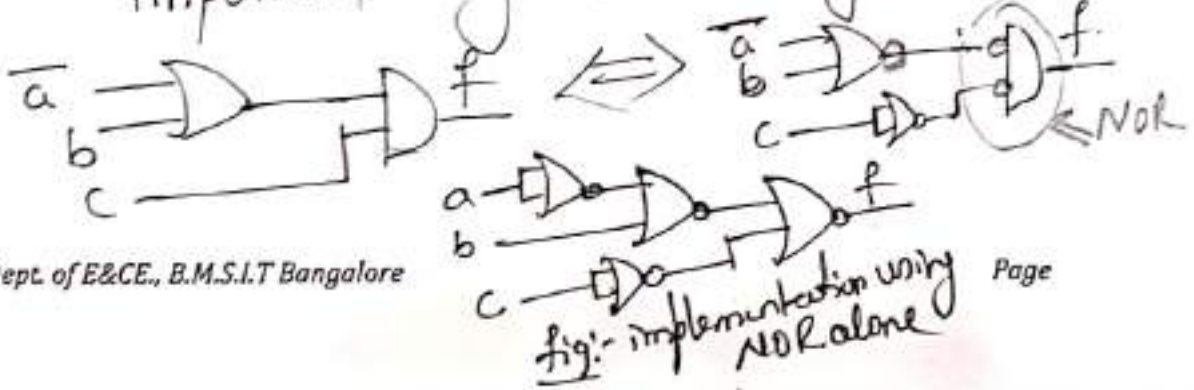


fig:- implementation using NOR alone

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Assignment

i. prove that $AB + A + AB = 0$.

ii. Simplify $\bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y} + x\bar{y}$

[Note:- Ans is $\bar{y}$]

iii. Simplify $ABC + AB\bar{C} + \bar{A}BC$

Ans:- $(AB + BC)$

iv. Simplify $\overline{\bar{x}y + xyz} + x(y + x\bar{y})$

Ans:- 0.

v. State and prove Demorgan theorem for 3 variable and 4 variables.

vi. State and prove Associative and distributive Law of Boolean algebra.

vii. Implement the following Boolean functions using
i. NAND gates only (NAND-NAND logic)
ii. NOR gates only (NOR-NOR logic)

a) $f = ab + b\bar{c} + cd + e$

b) $f = ab + bc + c\bar{a}$

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Assignment

i. prove that $AB + A + AB = 0$.

ii. Simplify $\bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y} + x\bar{y}$

[Note:- Ans is $\bar{y}$]

iii. Simplify $ABC + AB\bar{C} + \bar{A}BC$

Ans:- $(AB + BC)$

iv. Simplify $\overline{\bar{x}y + xyz} + x(y + x\bar{y})$

Ans:- 0.

v. State and prove Demorgan theorem for 3 variable and 4 variables.

vi. State and prove Associative and distributive Law of Boolean algebra.

vii. Implement the following Boolean functions using
i. NAND gates only (NAND-NAND logic)
ii. NOR gates only (NOR-NOR logic)

a) $f = ab + b\bar{c} + cd + e$

b) $f = ab + bc + c\bar{a}$

Half adder :-

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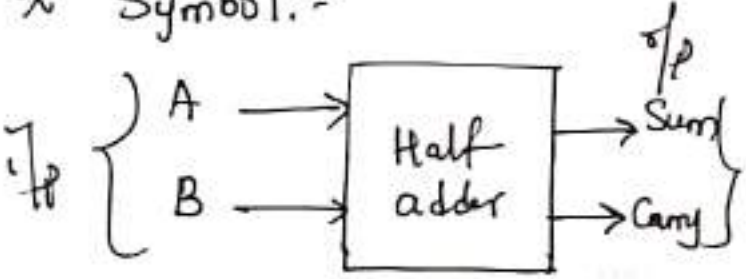
* Half adder is a combinational Circuit that performs the addition of two bits. this Circuit needs two binary inputs and two binary outputs.

* Symbol:-



Truth table

i/p		o/p	
A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

* Boolean Expressions

$$Sum = \bar{a}b + a\bar{b} = a \oplus b$$
$$Cout = ab$$

* Implementation of Half adder using Basic gates (fig a)

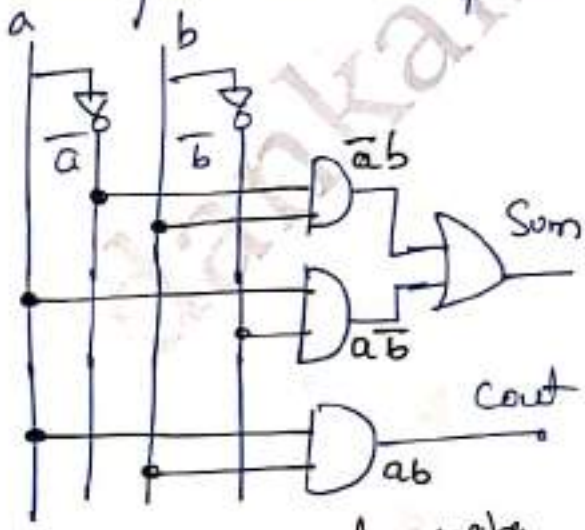


fig a: implementation using Basic gates.

(or)

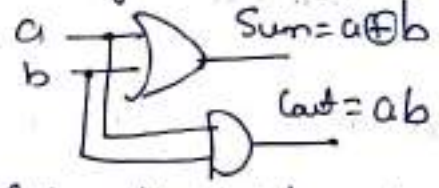


fig b. implementation using x-or & AND logic

drawback of HA :-

* Half adders have major limitation in that they cannot accept a carry bit from previous stage, meaning that they cannot be chained together to add multi-bit numbers.

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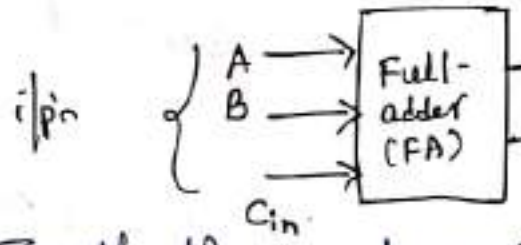
Topic 5.4 Combinational circuits: Half and Full adder, Multiplexer, Decoder.

Design Full adder circuit and implement it using basic gates. **(10Marks). Dec/Jan 2019/ (08 Marks) Dec-Jan 2020.**
With a neat circuit diagram and truth table, explain the full adder circuit. **(6 Marks) MQP-3**

Soln:- * A Fulladder is a Combinational Circuit that forms the arithmetic Sum of three input bits.



* it Consists of three inputs and two outputs.
* Two of the input variables, denoted by A, and B represents the two Significant bit to be added.
* third input Cin, represents the Carry from the previous Lower Significant position.
* Truth table of Full-adder

Decimal value	Inputs			outputs	
	A	B	Cin	Sum	Cout
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

$Sum = \sum m(1, 2, 4, 7)$

$Cout = \sum m(3, 5, 6, 7)$

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Boolean expression for Sum

$$Sum = \bar{a}\bar{b}C_{in} + \bar{a}b\bar{C}_{in} + a\bar{b}\bar{C}_{in} + abC_{in} \leftarrow (1)$$

$$= C_{in}(\bar{a}\bar{b} + ab) + \bar{C}_{in}(\bar{a}b + a\bar{b})$$

$$= C_{in}(a \odot b) + \bar{C}_{in}(a \oplus b)$$

W.k.t $a \odot b = \overline{a \oplus b}$

Say wt $x = a \oplus b \Rightarrow a \odot b = \bar{x}$

$$Sum = C_{in}\bar{x} + C_{in}x$$

$$Sum = C_{in} \oplus x = C_{in} \oplus a \oplus b$$

$$\Rightarrow (a) \quad \boxed{Sum = a \oplus b \oplus C_{in}} \leftarrow (1a)$$

Boolean Expression for Cout:-

$$C_{out} = \bar{a}bC_{in} + a\bar{b}C_{in} + ab\bar{C}_{in} + abC_{in}$$

$$= \bar{a}bC_{in} + a\bar{b}C_{in} + abC_{in} + ab\bar{C}_{in} + abC_{in} + abC_{in}$$

↑ added newly by us $\quad x + x = x$ itself.

By rearranging the terms

$$= \bar{a}bC_{in} + abC_{in} + a\bar{b}C_{in} + abC_{in} + ab\bar{C}_{in} + abC_{in}$$

$$= (\bar{a} + a)bC_{in} + aC_{in}(\bar{b} + b) + ab(\bar{C}_{in} + C_{in})$$

$$\boxed{C_{out} = bC_{in} + aC_{in} + ab} \leftarrow (2)$$

Logic diagram :-

$$Sum = \bar{a}\,\bar{b}\,C_{in} + \bar{a}\,b\,\bar{C}_{in} + a\bar{b}\,\bar{C}_{in} + abC_{in} \leftarrow (1)$$

$$C_{out} = ab + bC_{in} + C_{in}a \leftarrow (2)$$

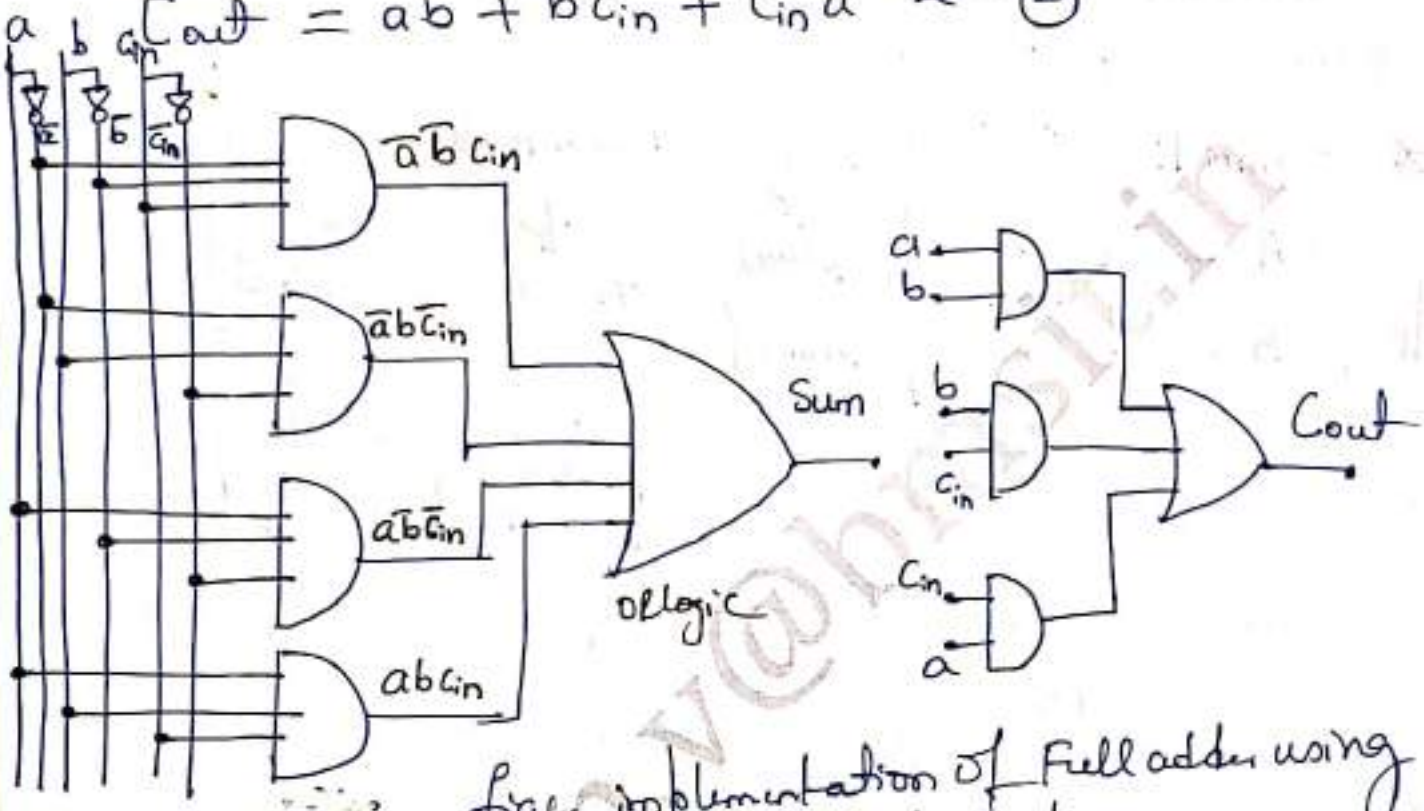
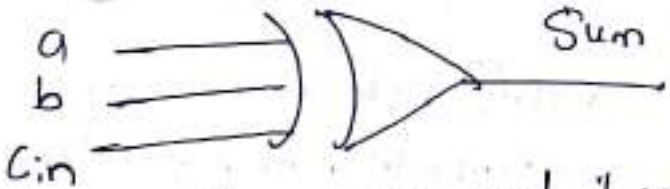


fig:- implementation of Full adder using Basic gates only.

Note:-

alternative diagram for Sum;-

using eq^n (1a) i.e $Sum = a \oplus b \oplus C_{in}$



Note:- In the question if it is Mentioned implement using basic gates. then don't use Ex-OR gate for Sum.

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Realize/Implment full adder using two half adders. (04 Marks) Dec/Jan 2019./ (6 Marks) MQP-1

Design full adder circuit using three variables and implement it using two half adders. (8 Marks) MQP-2

Soln:- Note:- Representation of F.A (Refer previous Section.)
Theory
and Truth table
Derivation of Sum & Carry Expression's i.e

⇒ after obtaining Sum and Carry expression.

$$Sum = \bar{a}\bar{b}C_{in} + \bar{a}b\bar{C}_{in} + a\bar{b}\bar{C}_{in} + abC_{in}$$

$$Sum = (\bar{a}\bar{b} + ab)C_{in} + (\bar{a}b + a\bar{b})\bar{C}_{in}$$

$$= (a \odot b)C_{in} + (a \oplus b)\bar{C}_{in}$$

$$Sum = \overline{(a \oplus b)}C_{in} + (a \oplus b)\bar{C}_{in}$$

$$\boxed{Sum = a \oplus b \oplus C_{in}} \leftarrow (1)$$

The Carry output :-

$$C_{out} = \bar{a}bC_{in} + a\bar{b}C_{in} + abC_{in} + ab\bar{C}_{in}$$

$$= C_{in}(\bar{a}b + a\bar{b}) + ab(C_{in} + \bar{C}_{in})$$

$$\boxed{C_{out} = C_{in}\cdot(a \oplus b) + ab} \leftarrow (2)$$

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using eq^{n} ① & ②

i.e $Sum = C_{in} \oplus (a \oplus b)$

$Cout = C_{in} \cdot (a \oplus b) + ab$

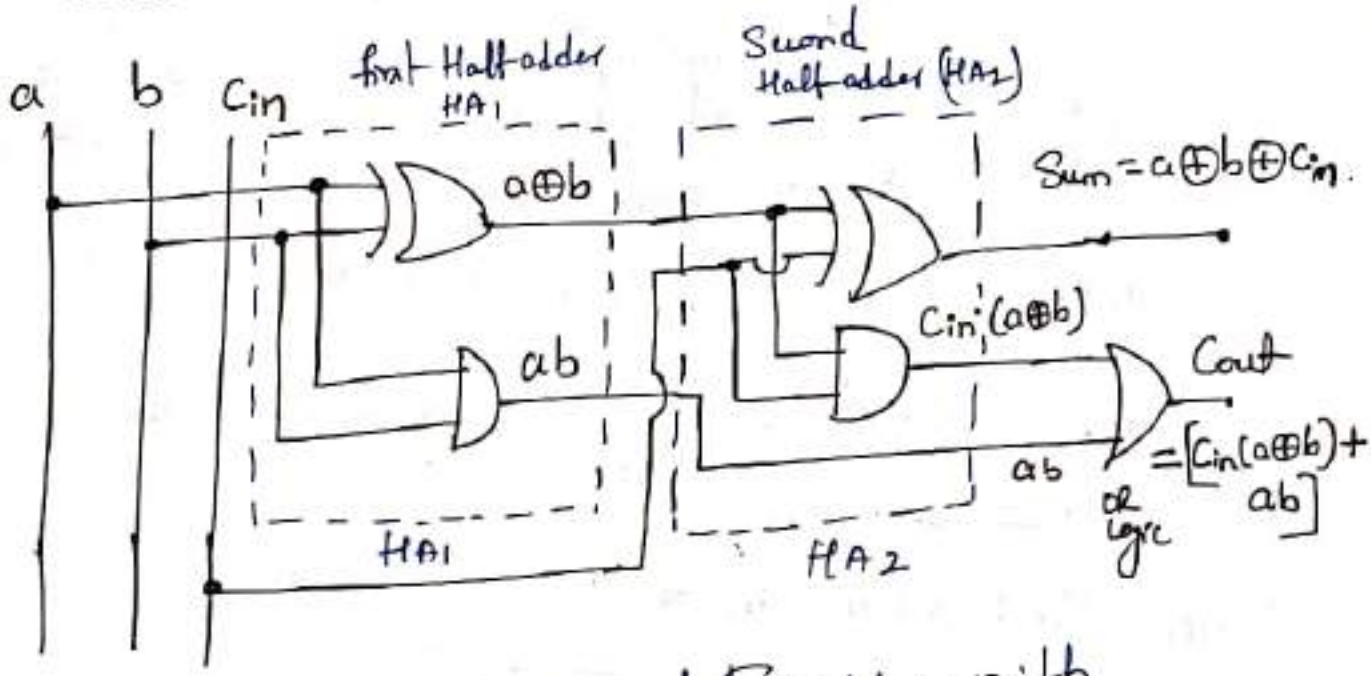
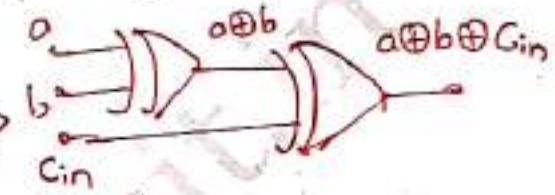


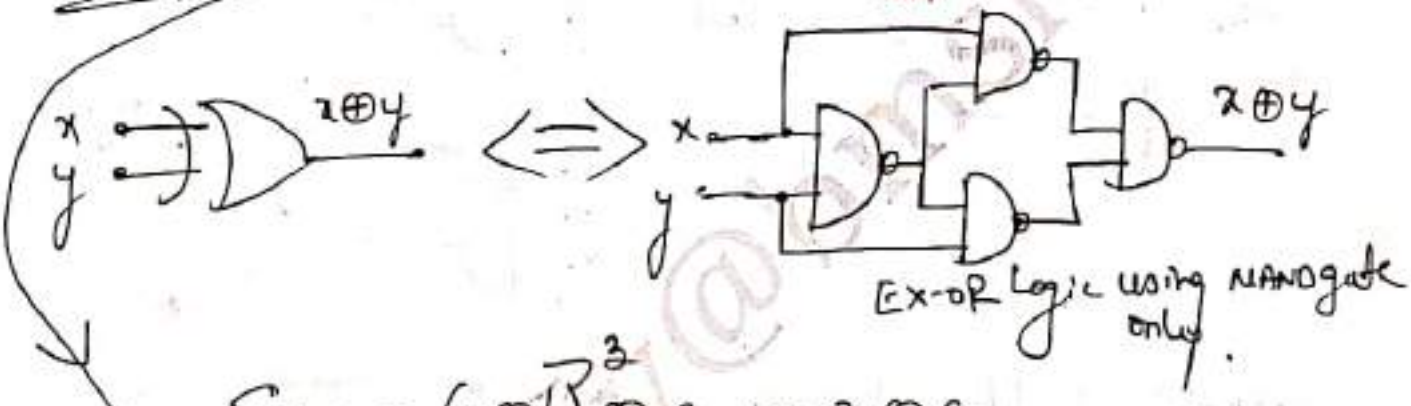
Fig. Implementation of Full adder with two - Half adders and an OR gate.

Realize Fulladder using NAND-gates

Soln:- Representation of FA ⇒ Refer previous Section -
theory, Truth table
derivation of Boolean Expressions of Sum and Carry



W.K.T $Sum = a \oplus b \oplus C_{in}$.



Ex-OR Logic using NAND gate only.

$Sum = (a \oplus b) \oplus C_{in} = z \oplus C_{in}$.

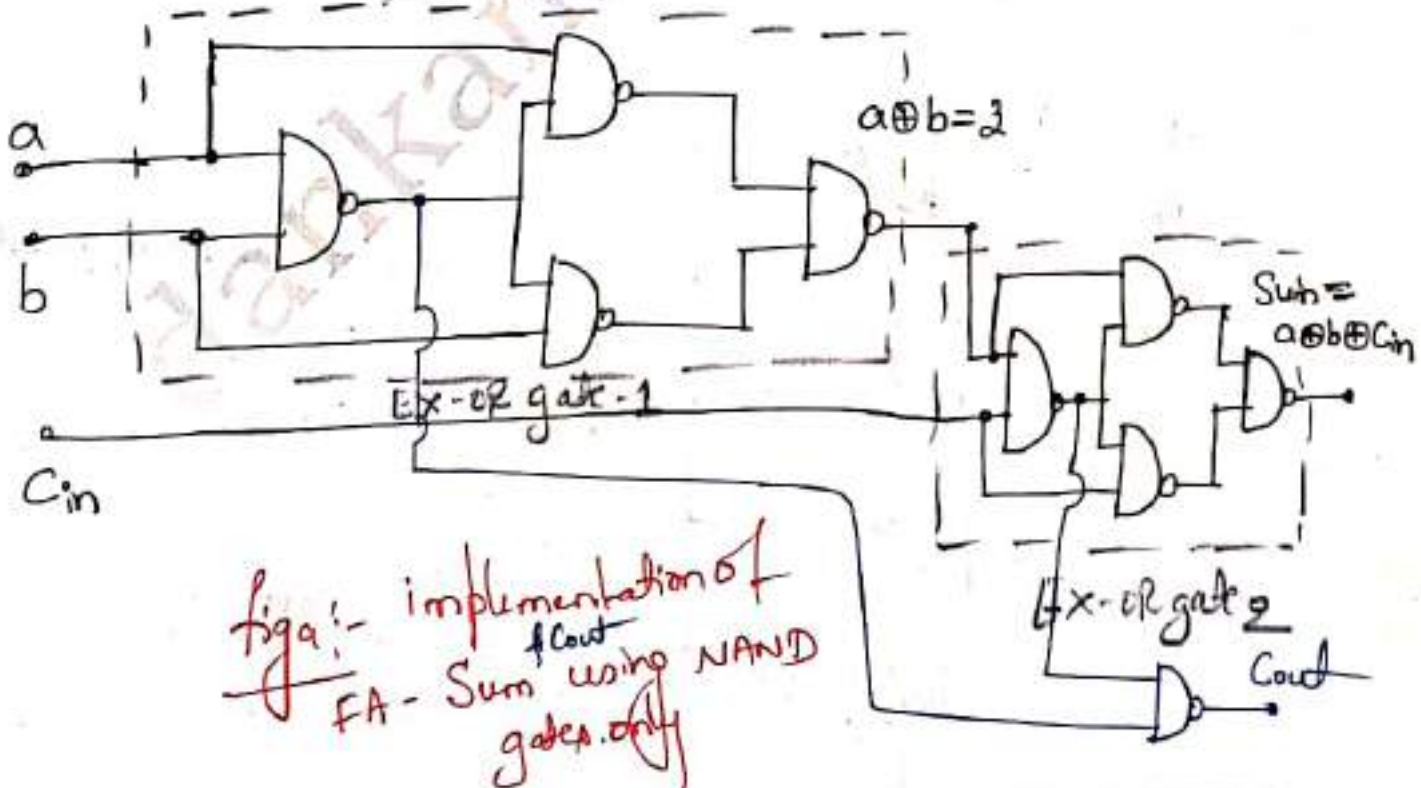
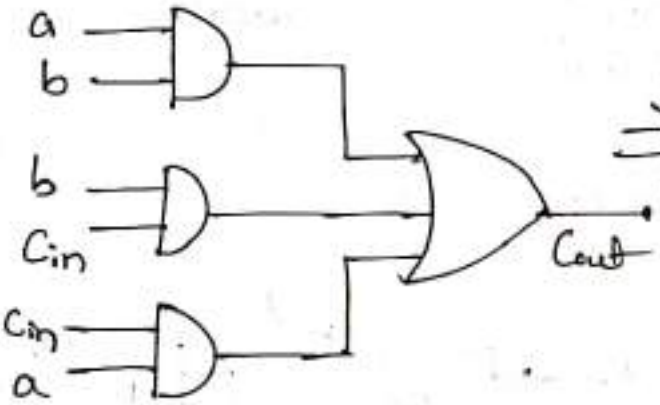


fig:- implementation of FA - Sum & Cout using NAND gates only

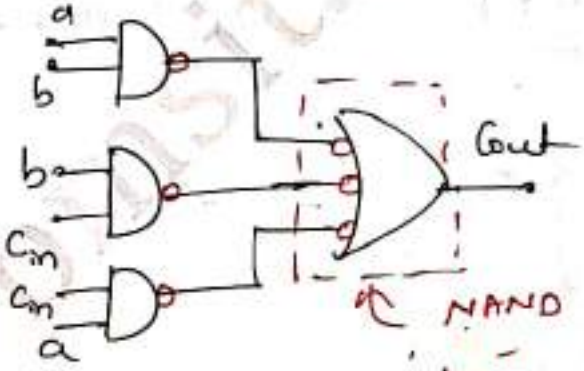
the Carry out

$$C_{out} = ab + bC_{in} + C_{in}a \Leftarrow \text{SOP expression}$$

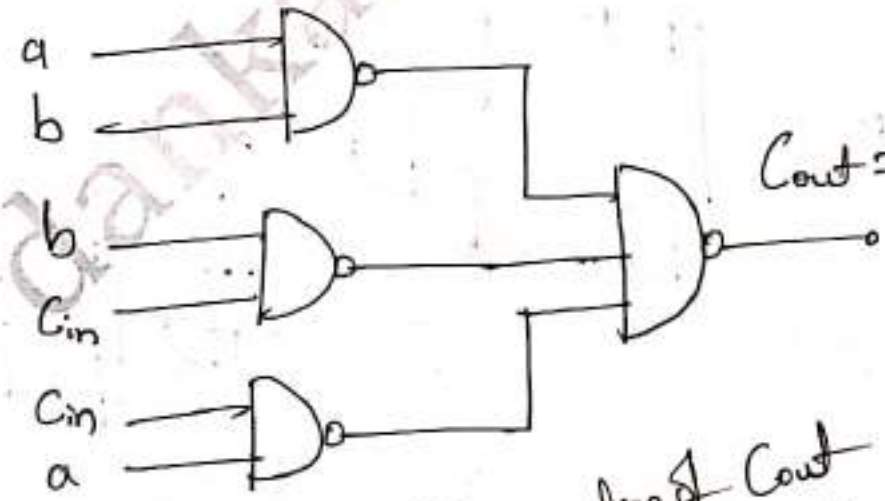
Step1. implement using AND-OR logic



Step2:- include bubble at output of AND gate & input of OR gate.



Step3:- Implementation of NAND gates alone.

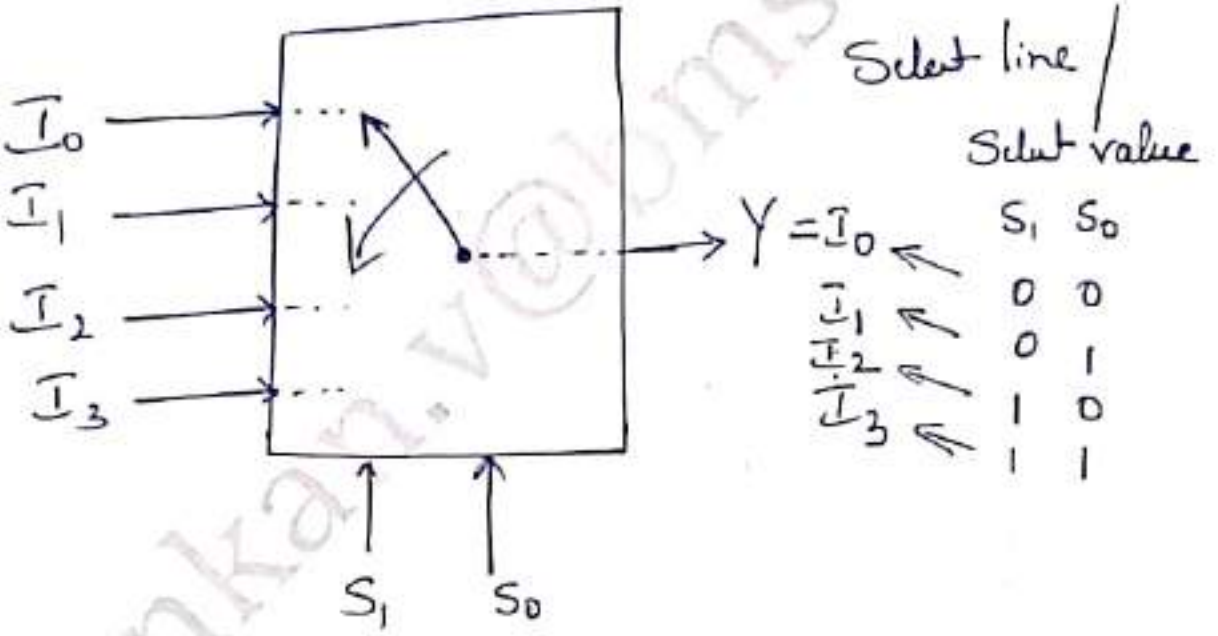


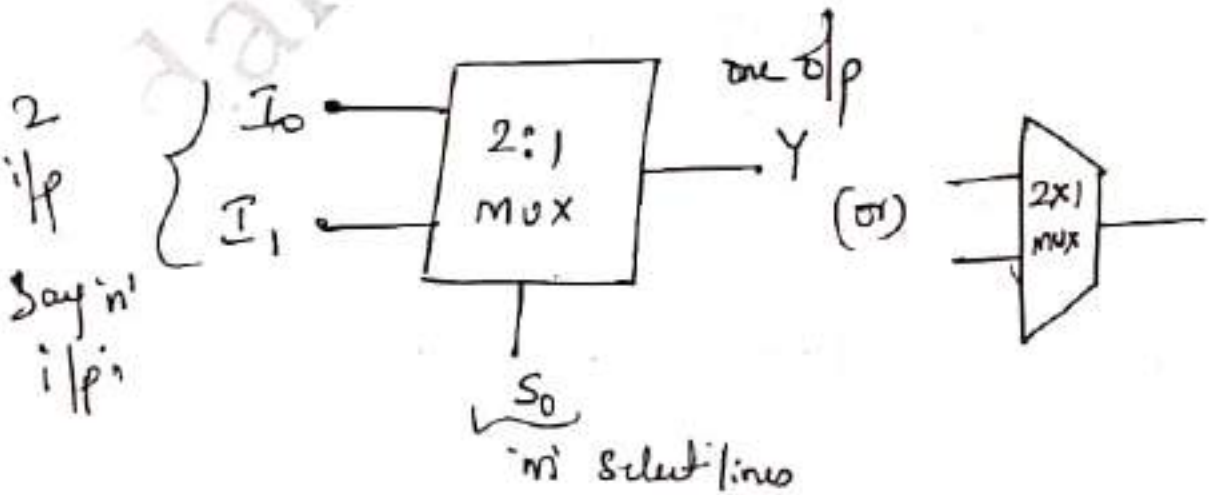
$C_{out} = ab + bC_{in} + C_{in}a$

Fig:- Realization of Cout using NAND gates only.

Multiplexer's (MUX)

* it is combinational Circuit that selects binary information from one of many input lines and directs it to output line.
* it is Simply a "Data Selector"





Relation b/w no. of i/p lines (n) and no. of select lines (m) is

$$\Rightarrow \boxed{n = 2^m}$$ ← no of select lines

no. of i/p lines

$\log_2$ on both side

$$\Rightarrow \log_2 n = \log_2 2^m$$

$$\Rightarrow \log_2 n = (\log_2 2) \cdot m \quad (\log_2 2 = 1)$$

$$\therefore \boxed{m = \log_2 n}$$

for $n = 4$

$$m = \log_2 4 = \log_2 2^2 = 2 \log_2 2 \quad (\log_2 2 = 1)$$

$$\therefore \boxed{m = 2}$$

* Data selector diff are available in the form of IC's.

(MSI) → IC's.

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→ Refer Next Section.

What is multiplexer? Implement 8:1 multiplexer using basic gates. **(08 Marks) Dec/Jan 2019.**

Soln:- Defn:- Multiplexer, it is a Combinational Circuit that Selects binary information from one of many input lines and directs it to output line.

ie it is simply a "DATA SELECTOR".

Advantages of MUX

i. it Reduces no. of wires. → by no of gates are reduced.

ii. Reduces Circuit Complexity and cost. (Since no of wires & Gates are reduced ∴ Cost ↓)

iii. Implementation of Various Circuits using MUX.

Types:-

2:1 MUX, 4:1 MUX, 8:1 MUX, 16:1 MUX and 32:1 MUX

no of Select lines	1	2	3	4	5

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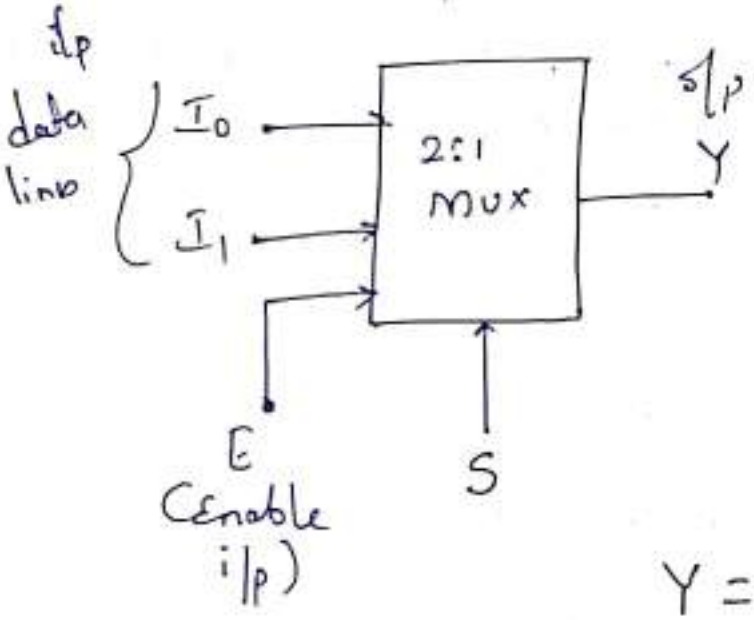
2:1 mux :-



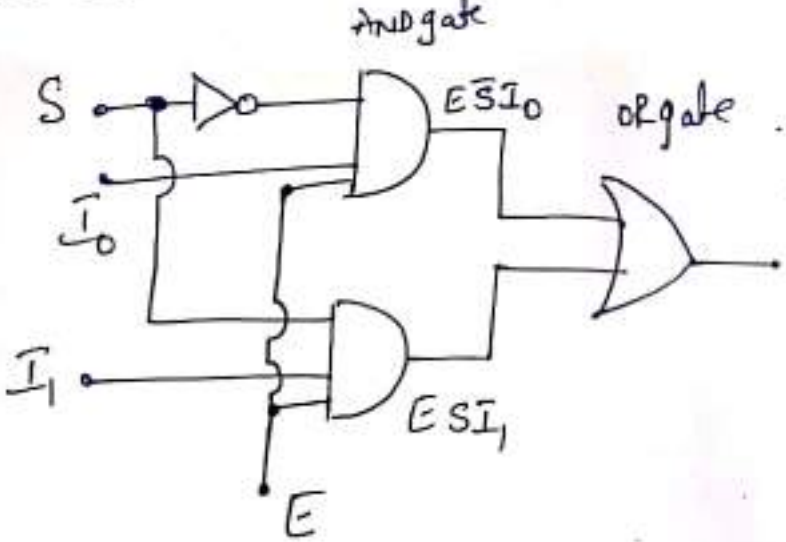
Truth table

E	S	Y
0	X	0
1	0	I_0
1	1	I_1

$$Y = E \cdot \bar{S}\, I_0 + E \cdot S \cdot I_1$$

$$\boxed{Y = E \cdot (\bar{S} \cdot I_0 + S \cdot I_1)}$$

Implementation of 2:1 mux :-



$$Y = E \cdot (\bar{S} I_0 + S \cdot I_1)$$

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→ Refer previous page.

What is a multiplexer? Explain the working of 4:1 multiplexer. (6 Marks) MQP-1

Soln:- 4X1 multiplexer

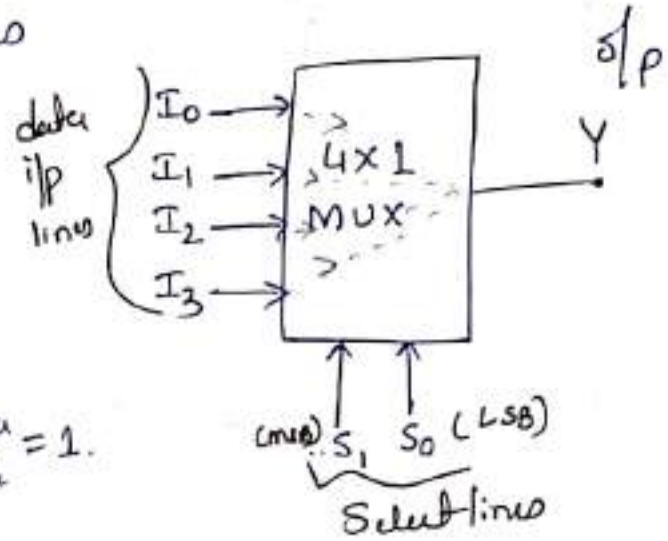
n = 4 : no of data lines

$m = \log_2 n$

$m = \log_2 4 = 2\log_2 2$

$m = 2$

note: $\log_a a = 1$.



Truth table:-

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \bar{S_1}\bar{S_0}I_0 + \bar{S_1}S_0I_1 + S_1\bar{S_0}I_2 + S_1S_0I_3$$

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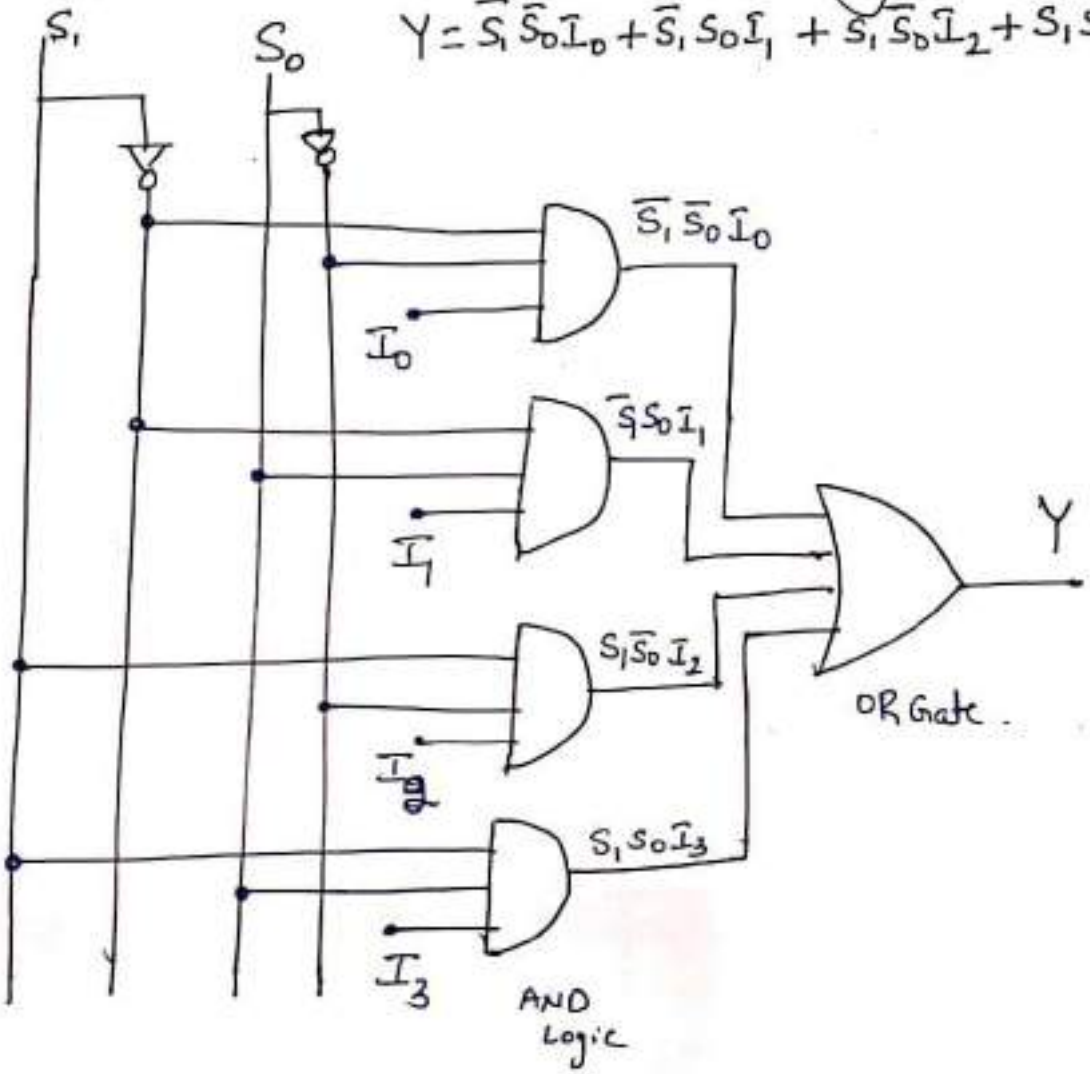
Implementation of 4:1 mux using Basic Gates.

$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$



Question. → Refer previous pages.

What is Multiplexer ? Implement 8:1 mux using basic gates. (08 Marks) Dec/Jan 2019.

Solution:

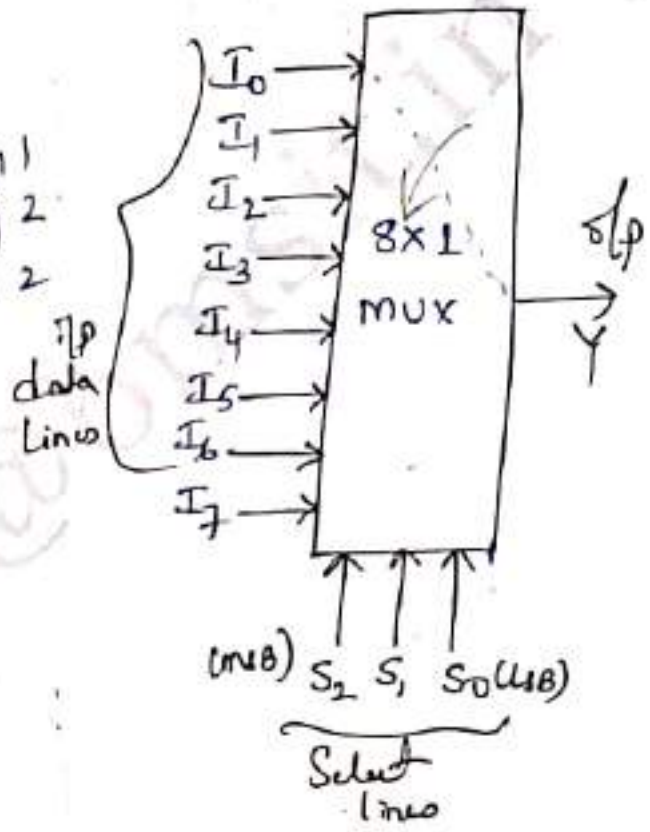
8 × 1 Multiplexer

$n = 8 = 2^3 = 2^m$

$\boxed{m = 3}$

(a) $m = \log_2 n = \log_2 2^3 = 3 \log_2 2$, $\log_2 2 = 1$

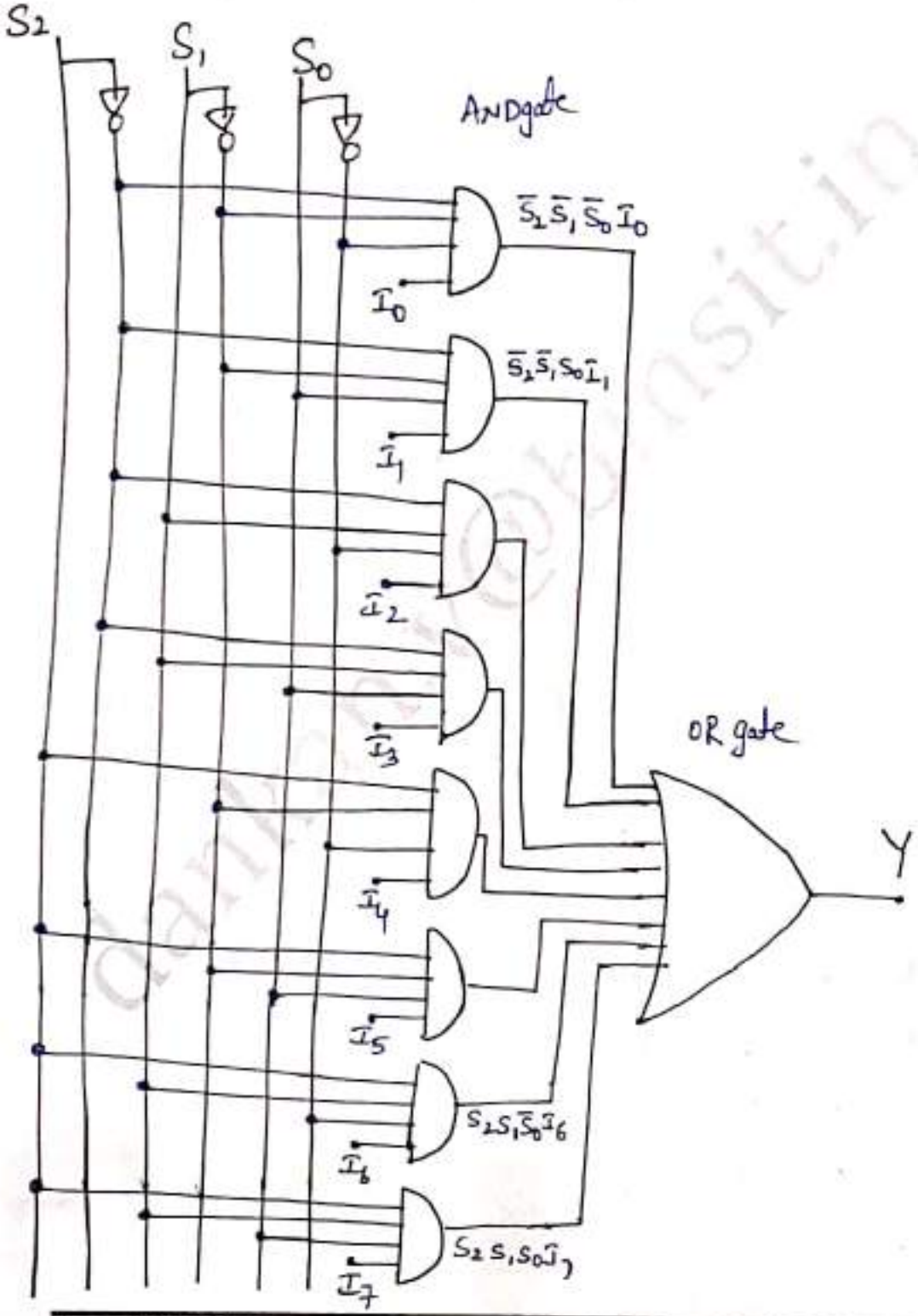
$\therefore \boxed{m = 3}$



Truth table:-

S_2	S_1	S_0	o/p Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

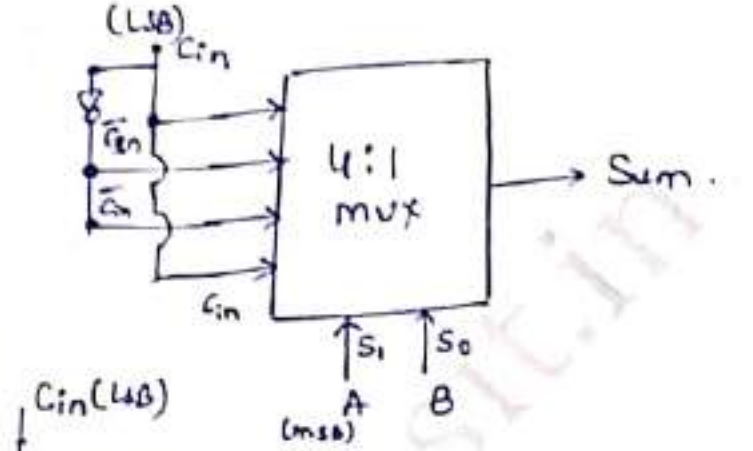
$$Y = \bar{S}_2\bar{S}_1\bar{S}_0 I_0 + \bar{S}_2\bar{S}_1 S_0 I_1 + \bar{S}_2 S_1\bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 + S_2\bar{S}_1\bar{S}_0 I_4 + S_2\bar{S}_1 S_0 I_5 + S_2 S_1\bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

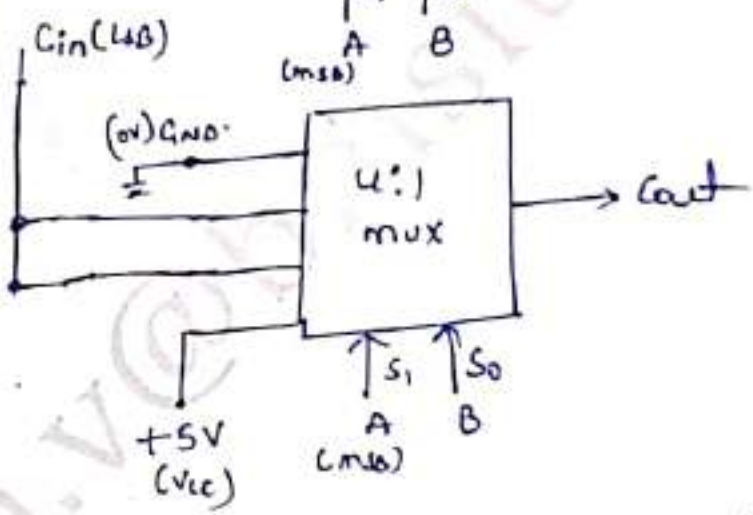


Implementation of Full adder using i) 4:1 mux ii) 8:1 mux

Soln: i) 4:1 mux

	a (I4)	b (I2)	Cin (LSB)	S (I1)	Cout (I0)
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

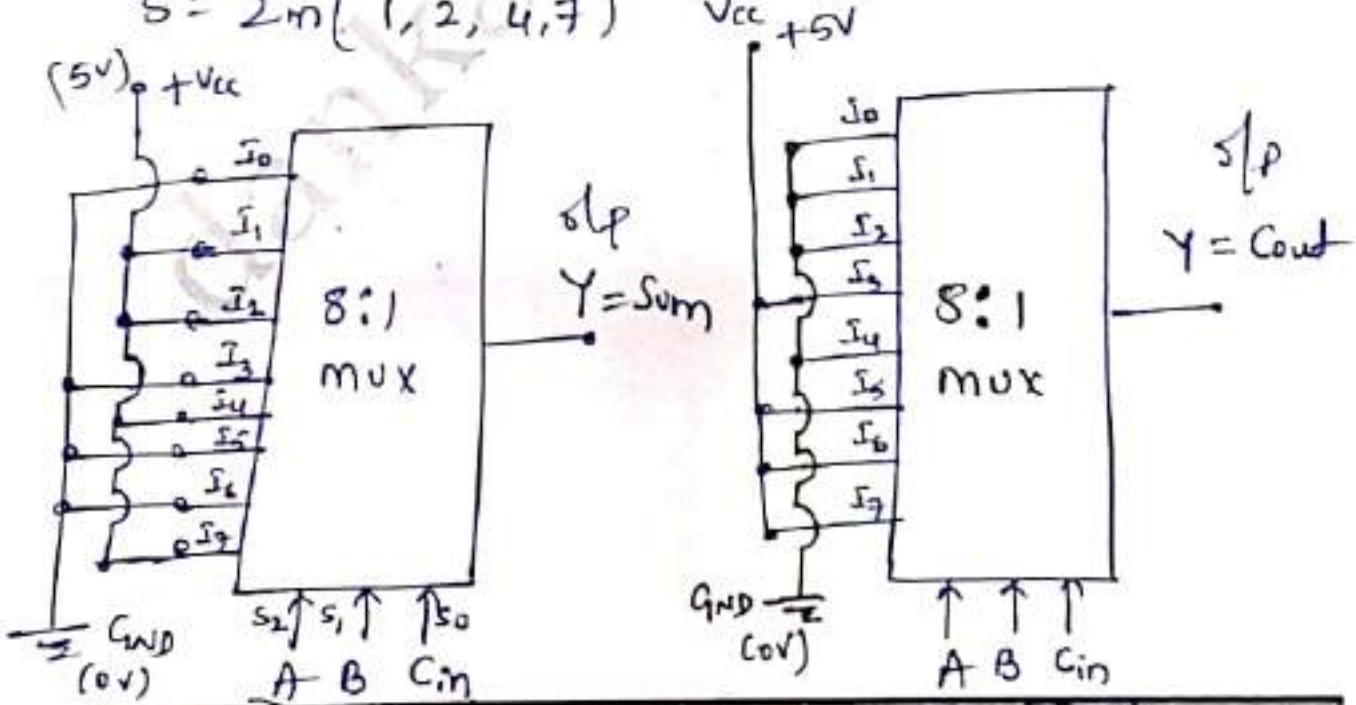




ii) using 8:1 mux

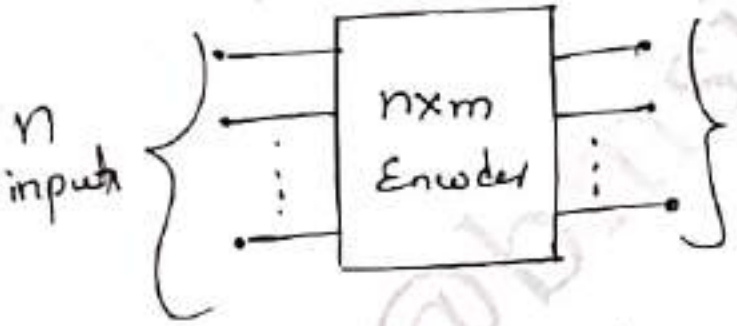
$S = \Sigma m(1, 2, 4, 7)$

$Cout = \Sigma m(3, 5, 6, 7)$

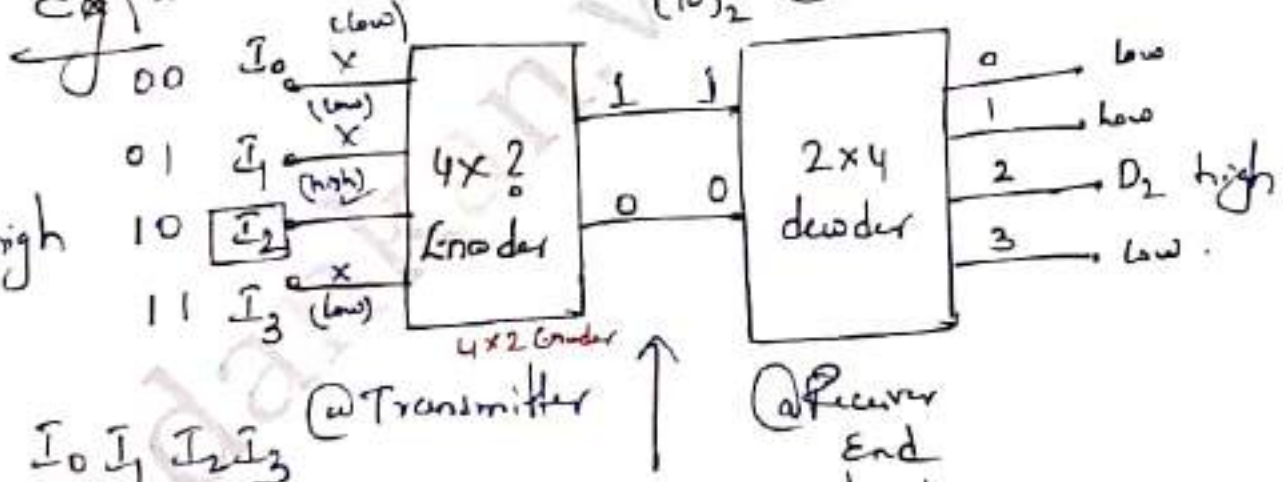


Introduction to Encoders and Decoders

* They are Combinational Circuits.
* Encoders have "n" input and "m" output.
* Function of decoder is opposite to Encoder.



Eg:-



$I_0\ I_1\ I_2\ I_3$

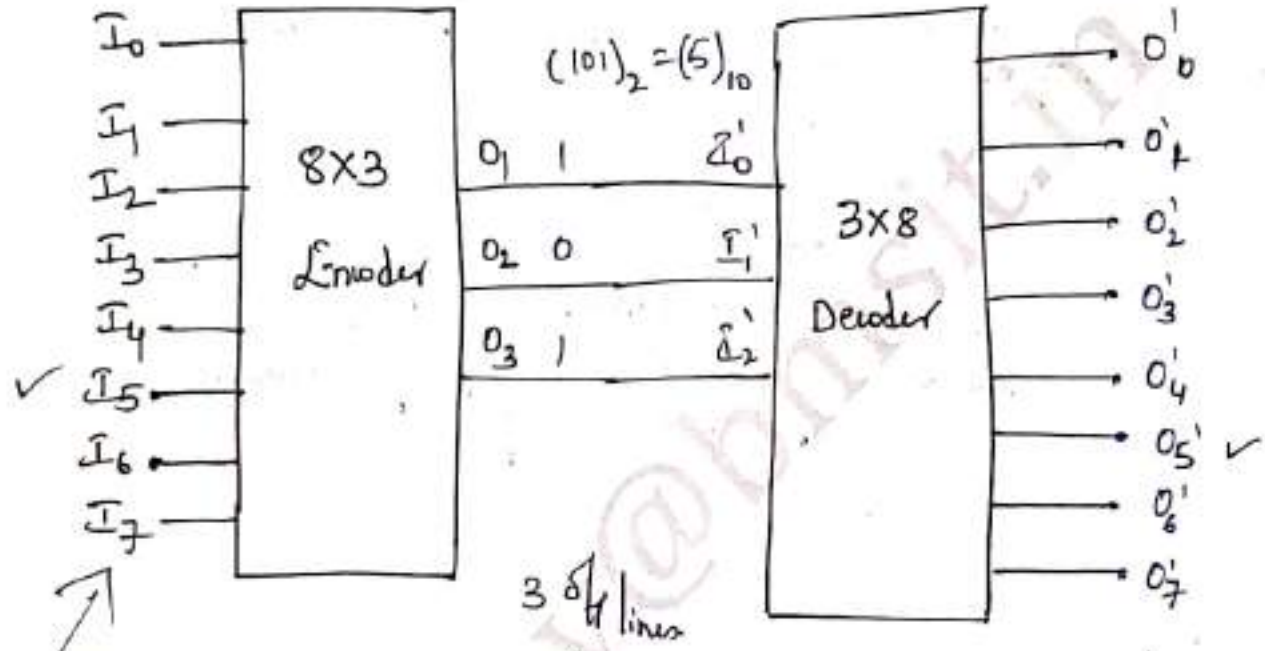
0 0 1 0

4 bit (four lines) $\Rightarrow$ 2 lines $\Rightarrow$ (0 0 1 0)

$n = 4$

$n = 2^2 = 2^m$

$n = 2^m$ — m: no. of o/p lines. Encoder; n: no. of i/p lines



$n = 8 = 2^3$

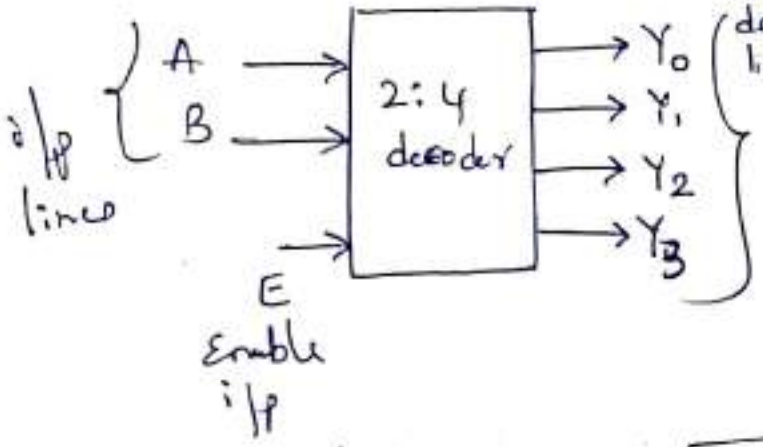
Applications of Decoder :-

i. used in Communication System. ie Encoders are used at Transmitter end and Decoders at Receiver end.

ii. used to implement Boolean functions.

iii. Decoders are greatly used in applications where the particular output (or) group of outputs to be activated only on the occurrence of a specific combination of input levels.

2:4 Decoder

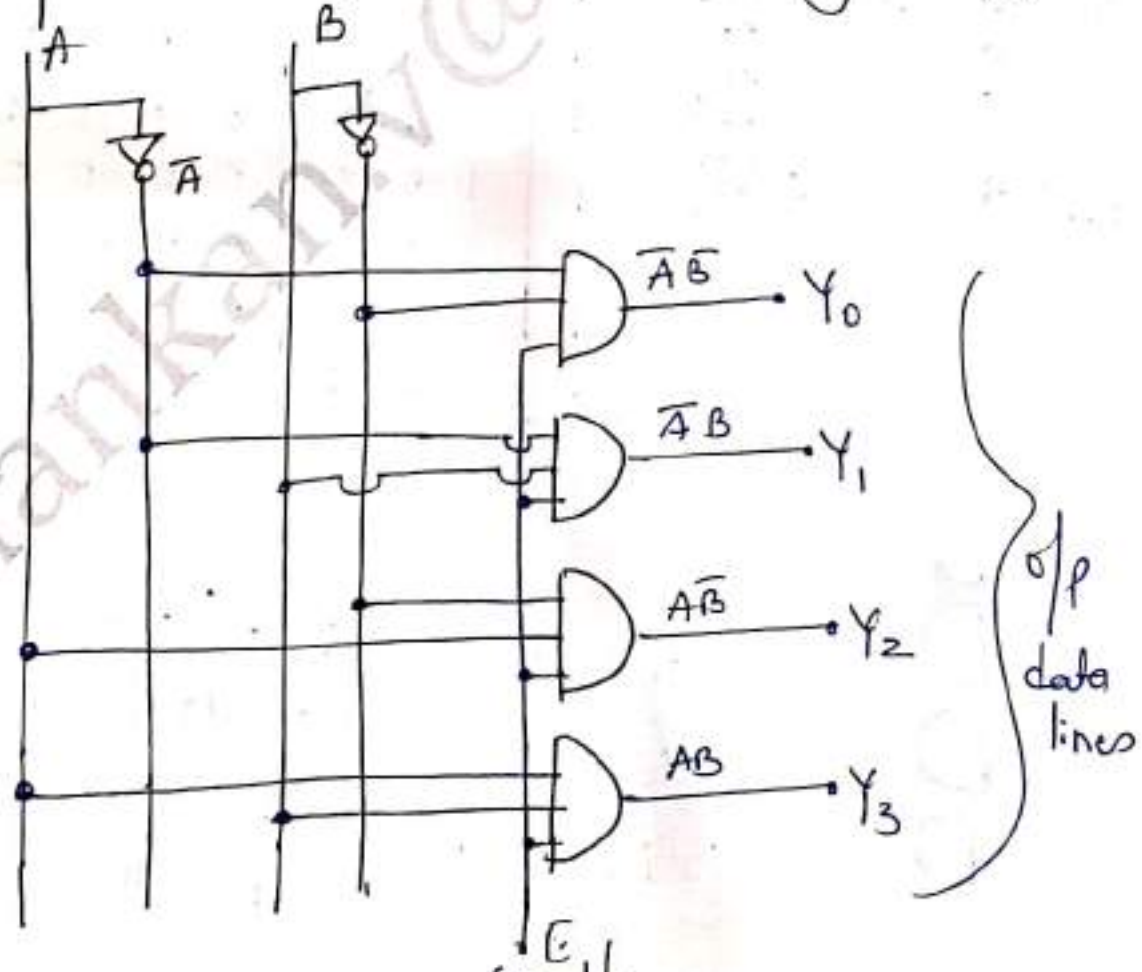


Truth table

E	i/p A	i/p B	o/p Y_0	o/p Y_1	o/p Y_2	o/p Y_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Boolean Expressions:- $Y_0 = \bar{A}\,\bar{B}\,E + \bar{A}BE + A\bar{B}E + ABE$

Implementation of 2:4 decoder using Basic gates



$m : 2^m$

Decoder :- (n : m decoder)

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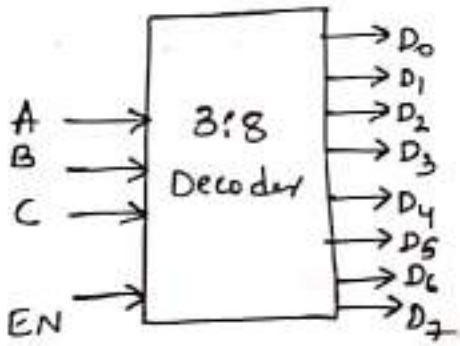
* Decoder is a combinational circuit that has 'm' input lines and maximum of $n = 2^m$ output lines.
* The decoder detects a particular code.
* One of these outputs will be active high based on the combination of inputs present, when the decoder is Enable.

3:8 Decoder :-



Truth table :-

i/ps				o/p							
E	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Boolean Expressions :-

$Y_0 = \bar{A}\bar{B}\bar{C}$

$Y_1 = \bar{A}\bar{B}C$

$Y_2 = \bar{A}B\bar{C}$

$Y_3 = A\bar{B}\bar{C}$

$Y_4 = A\bar{B}\bar{C}$

$Y_5 = A\bar{B}C$

$Y_6 = AB\bar{C}$

$Y_7 = ABC$

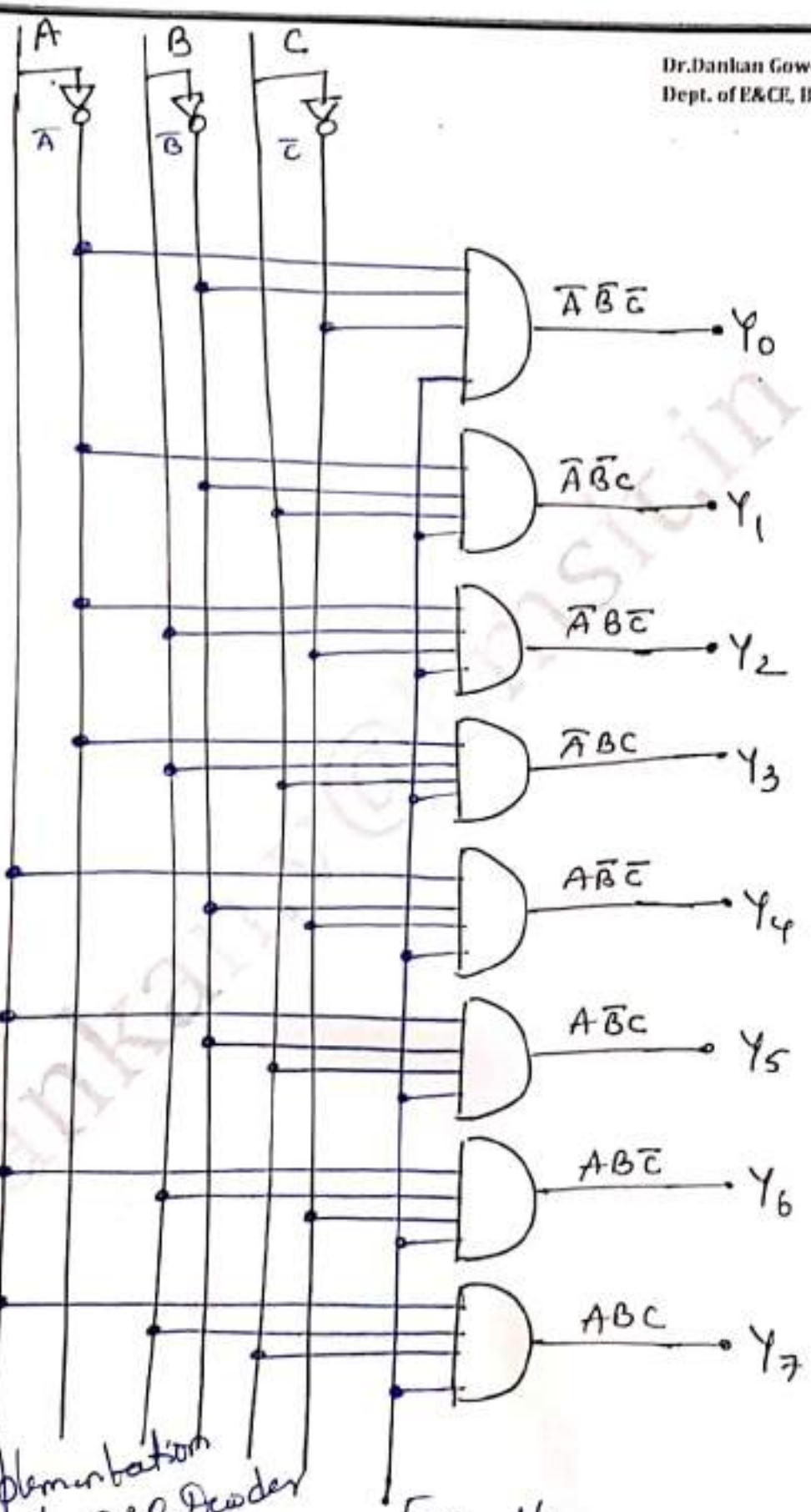


Fig: Implementation of 3:8 Decoder using Basic Gates.

Combinational Logic Design using Decoders

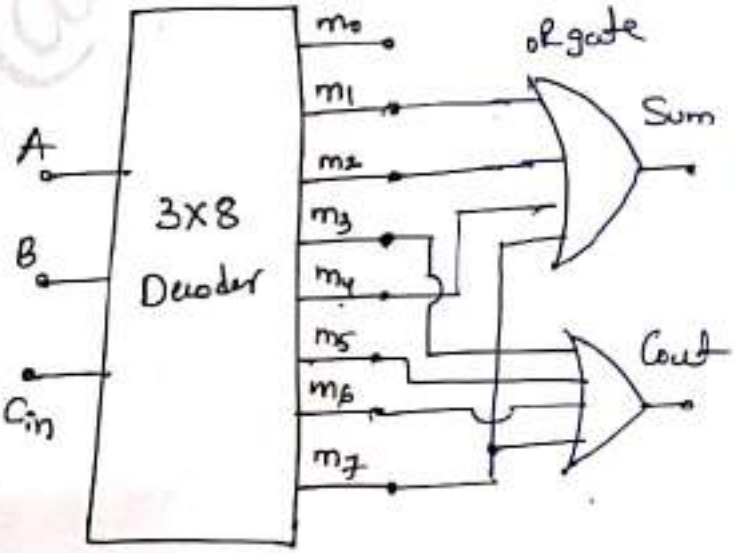
Full adder implementation using Decoder

Truth table of FA

	A	B	C_{in}	S	C_{out}	
0	0	0	0	0	0	m_0
1	0	0	1	1	0	m_1
2	0	1	0	1	0	m_2
3	0	1	1	0	1	m_3
4	1	0	0	1	0	m_4
5	1	0	1	0	1	m_5
6	1	1	0	0	1	m_6
7	1	1	1	1	1	m_7

$$Sum = \sum_m (m_1, m_2, m_4, m_7)$$

$$C_{out} = \sum_m (m_3, m_5, m_6, m_7)$$



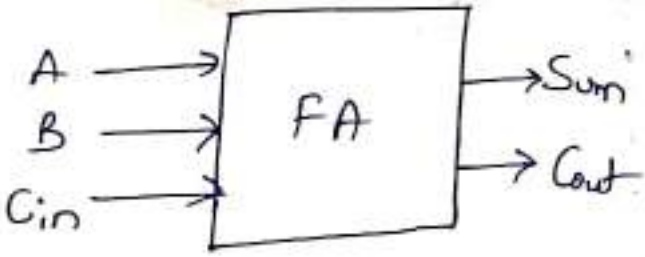
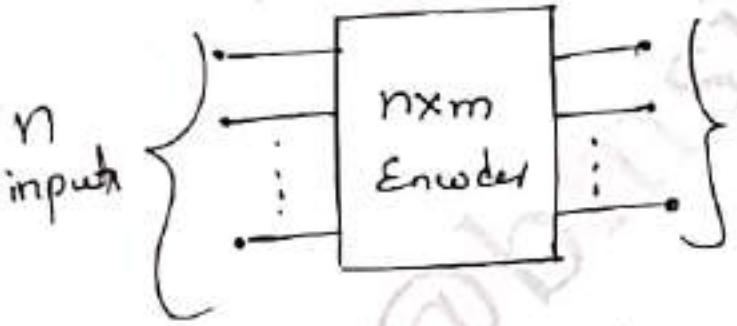


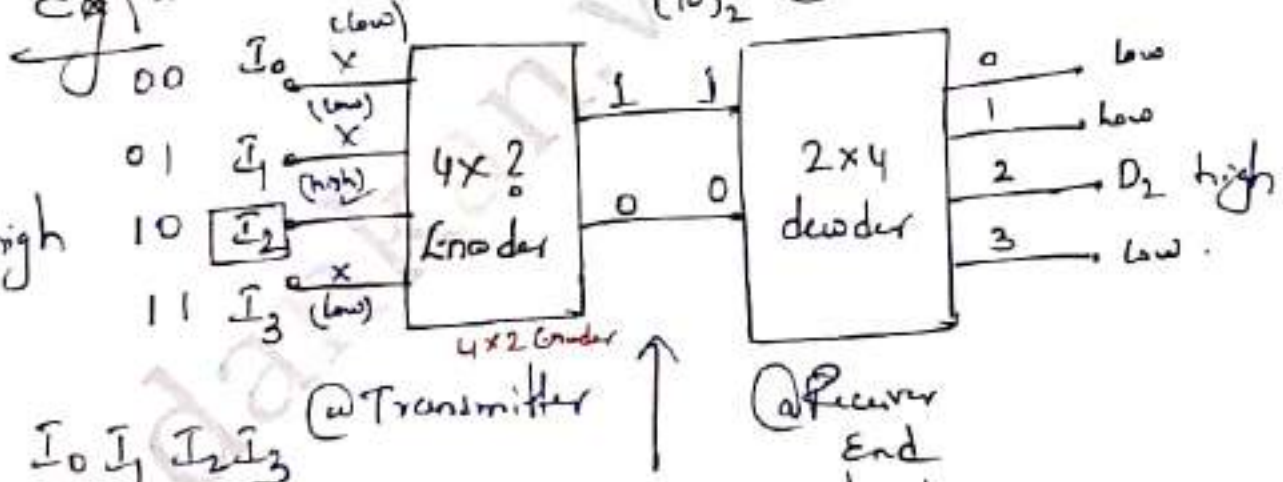
fig:- Full adder using 3×8 decoder.

Introduction to Encoders and Decoders

* They are Combinational Circuits.
* Encoders have "n" input and "m" output.
* Function of decoder is opposite to Encoder.



Eg:-



$I_0\ I_1\ I_2\ I_3$

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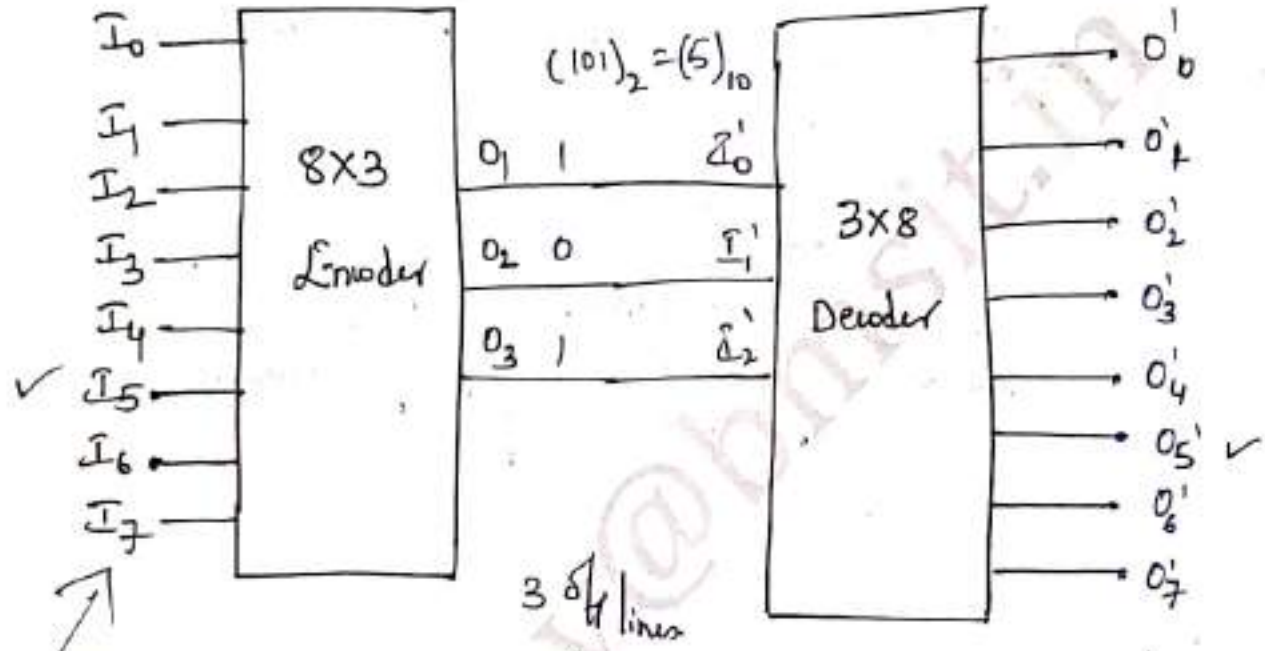

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Applications of Decoder :-

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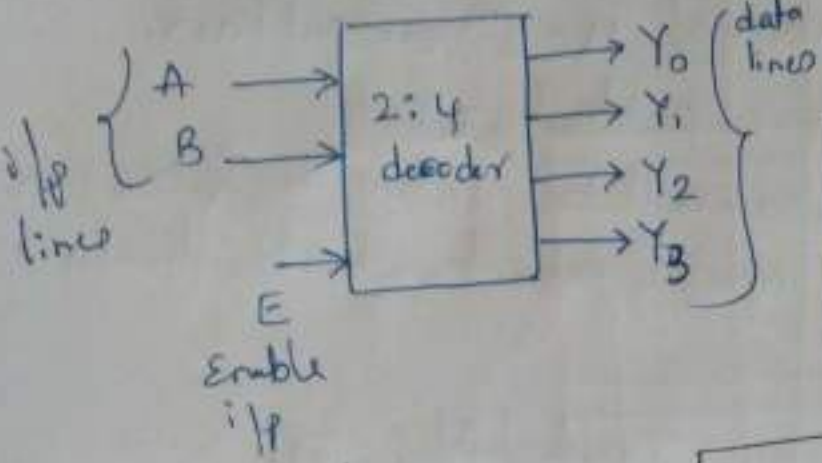
2:4 Decoder



Truth table

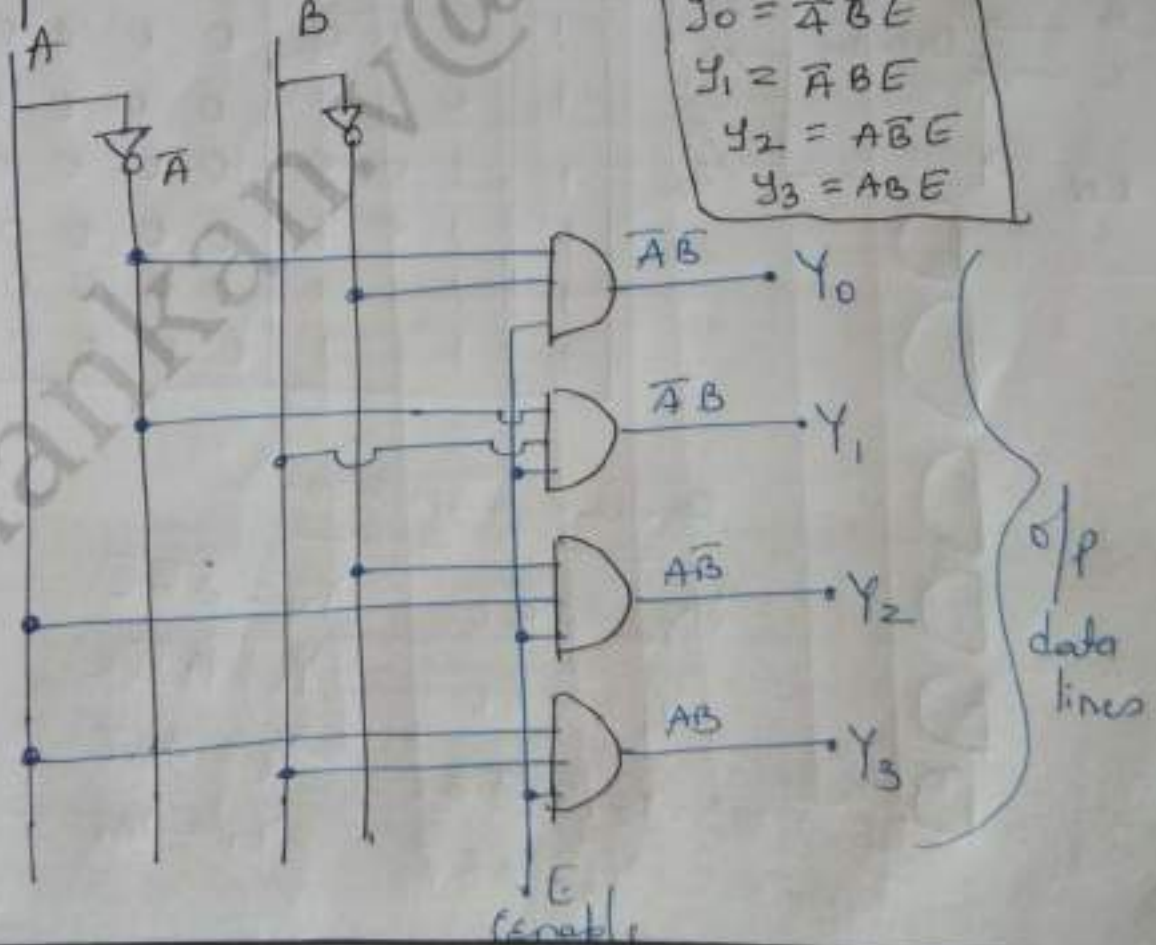
i/p			o/p			
E	A	B	Y_0	Y_1	Y_2	Y_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Boolean Expressions:-

$$Y \Rightarrow \underbrace{\bar{A}\bar{B}E}_{Y_0} \quad \underbrace{\bar{A}BE}_{Y_1} \quad \underbrace{A\bar{B}E}_{Y_2} \quad \underbrace{ABE}_{Y_3}$$

Implementation of 2:4 decoder using Basic gates

$Y_0 = \bar{A}\bar{B}E$
$Y_1 = \bar{A}BE$
$Y_2 = A\bar{B}E$
$Y_3 = ABE$



$m : 2^m$

Decoder :- (n : m decoder)

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* Decoder is a combinational circuit that has 'm' input lines and maximum of $n = 2^m$ output lines.
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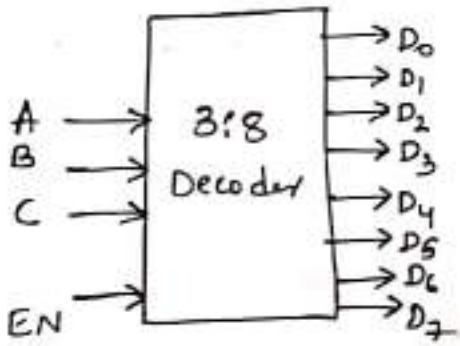

Truth table :-

i/ps				o/p							
E	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Boolean Expressions :-

$Y_0 = \bar{A}\bar{B}\bar{C}$

$Y_1 = \bar{A}\bar{B}C$

$Y_2 = \bar{A}B\bar{C}$

$Y_3 = A\bar{B}\bar{C}$

$Y_4 = A\bar{B}\bar{C}$

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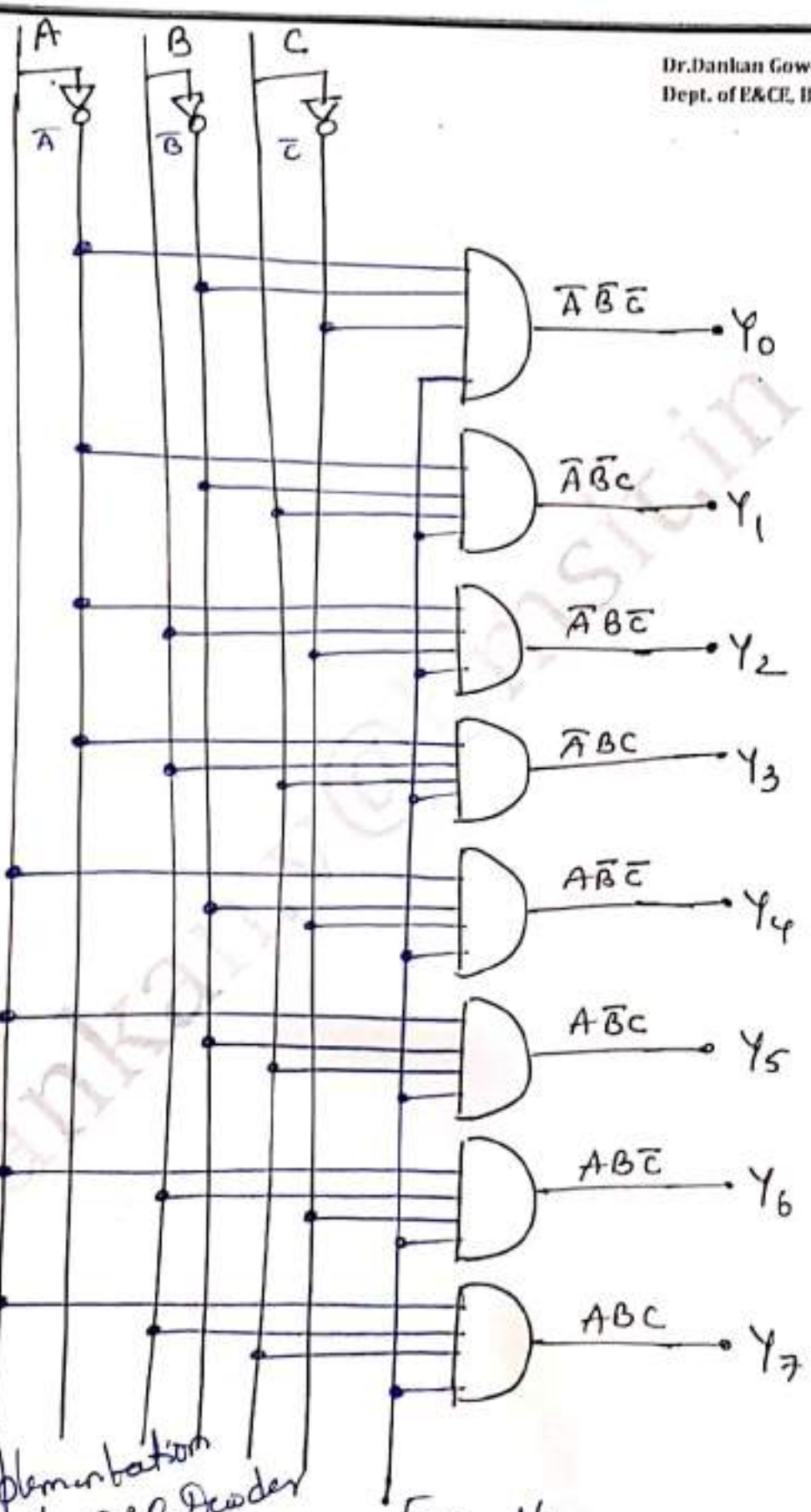


Fig: Implementation of 3:8 Decoder using Basic Gates.

Combinational Logic Design using Decoders

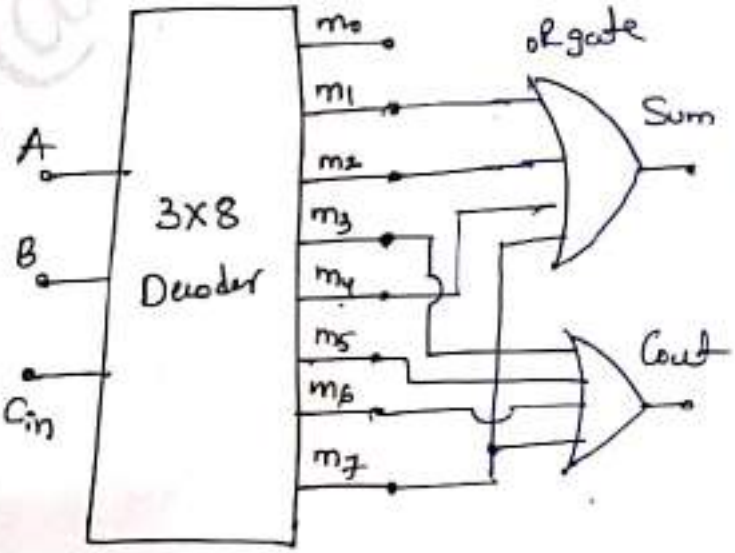
Full adder implementation using Decoder

Truth table of FA

	A	B	C_{in}	S	C_{out}	
0	0	0	0	0	0	m_0
1	0	0	1	1	0	m_1
2	0	1	0	1	0	m_2
3	0	1	1	0	1	m_3
4	1	0	0	1	0	m_4
5	1	0	1	0	1	m_5
6	1	1	0	0	1	m_6
7	1	1	1	1	1	m_7

$$Sum = \sum_m (m_1, m_2, m_4, m_7)$$

$$C_{out} = \sum_m (m_3, m_5, m_6, m_7)$$



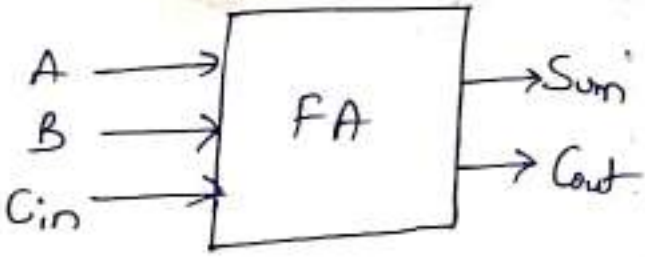


fig:- Full adder using 3×8 decoder.

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Flip - Flops

- Flip-flop is a bi-stable digital circuit, i.e., its outputs have two stable states : logic 1 and logic 0.
- It is a sequential circuit; it requires a clock signal to be applied at its inputs for operation.
- The Fig. shows the block diagram of a flip-flop. It has one or more inputs, two outputs and a clock input.

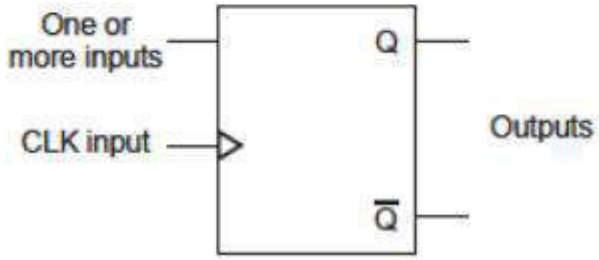

Fig. Flip-flop

- The Fig. shows the clock signal. It is a rectangular signal with 50 % duty cycle.

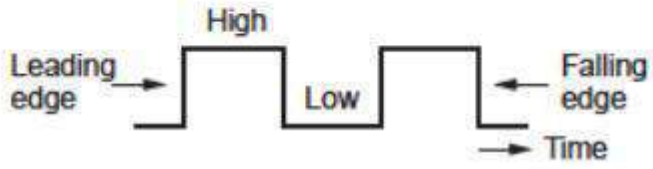

Fig.

- The flip-flop changes its outputs either at the leading edge of the clock signal or at the falling edge of the clock signal according to the status of flip-flop input present at that time.

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- The two outputs of flip-flop Q and $\overline{Q}$ always complements of each other.

➢ ***List various types of flip-flops.***

Different types of flip-flops are :

1. SR flip-flop 2. JK flip-flop
3. D flip-flop 4. T flip-flop
5. Master-slave flip-flop

➢ ***State various applications of flip-flops.***

Some of the important applications of flip-flops are :

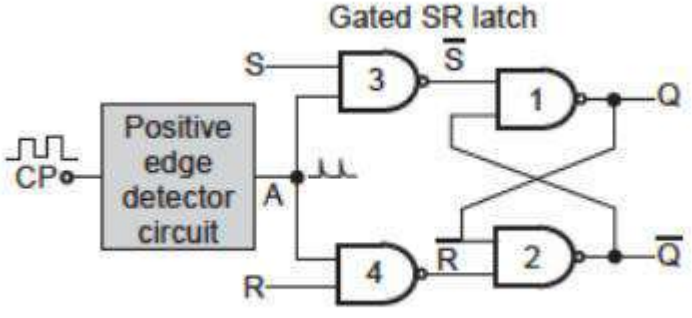
- It can be used as a memory element.
- It is used as a basic building block in sequential circuits such as counters and registers.
- It can be used as a delay element.

SR Flip - Flop

➢ ***Draw and explain the working of SR flip-flop. Give the truth table and characteristic equation of SR flip-flop.***

VTU : May-11, Dec.-11, 12 Marks 7

The Fig. shows the positive edge triggered clocked SR flip-flop.



(a) SR flip-flop using NAND gates

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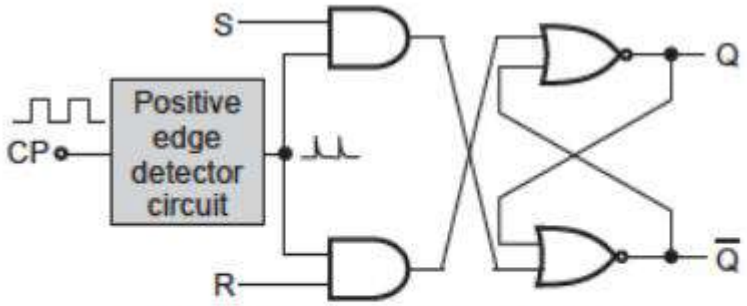
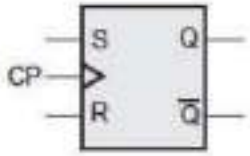


(b) SR flip-flop using NOR gates

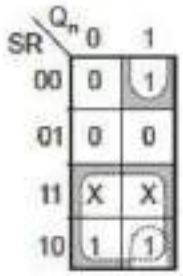
Fig. Clocked SR flip-flop



(a) Logic symbol

CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	No Change(NC)
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	X	Indeterminate
↑	1	1	1	X	
0	X	X	0	0	No Change(NC)
0	X	X	1	1	

(b) Truth table for positive edge clocked SR flip-flop



$Q_{n+1} = S + \overline{R}\,Q_n$

(c) Characteristic equation

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Operation

Case 1 : If S = R = 0 and the clock pulse is applied, the output do not change, i.e. $Q_{n+1} = Q_n$. This is indicated in the first row of the truth table.

Case 2 : If S = 0, R = 1 and the clock pulse is applied, $Q_{n+1} = 0$. This is indicated in the second row of the truth table.

Case 3 : If S = 1, R = 0 and the clock pulse is applied, $Q_{n+1} = 1$. This is indicated in the third row of the truth table.

Case 4 : If S = R = 1 and the clock pulse is applied, the state of the flip-flip is undefined and therefore is indicated as indeterminate in the fourth row of the truth table.

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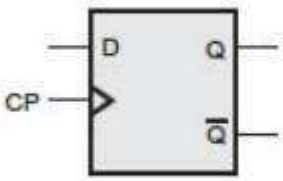
➢ *What is D flip - flop ?*

- In SR Flip-Flop, when both inputs are same the output either does not change or it is invalid (Inputs → 00, no change and inputs → 11, invalid).
- These input conditions can be avoided by making them complement of each other. This modified SR flip-flop is known as D flip-flop.
- The D input goes directly to the S input, and its complement is applied to the R input. Due to these connections, only two input conditions exists, either S = 0 and **R = 1 or S = 1 and R = 0**.

Truth Table : • The truth table for D flip-flop consider only these two conditions and it is as shown in the Fig. 7.16.5 (b).



CP	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n

Fig. (a) Logic symbol Fig. 7.16.5 (b) Truth table of D flip-flop

- Q_{n+1} function follows D input at the positive going edges of the clock pulses. Hence the characteristic equation for D flip-flop is Q_{n+1} = D.

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JK Flip - Flop

- The uncertainty in the state of an SR flip-flop when S = R = 1 can be eliminated by converting it into a JK flip-flop.
- The data inputs are J and K which are ANDed with Q and Q, respectively, to obtain S and R inputs, as shown in the Fig. Thus, $S = J \cdot \overline{Q}$ and $R = K \cdot Q$.

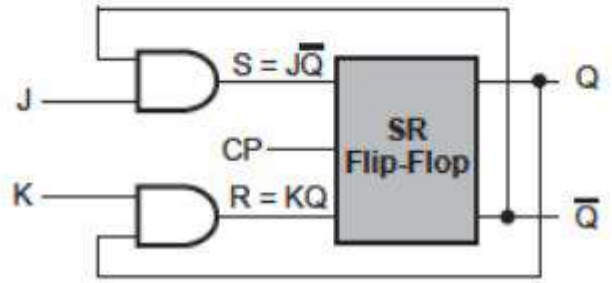

Fig. JK flip-flop using SR flip-flop

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Operation of JK Flip-Flop

Case 1 : J = K = 0

When J = K = 0, S = R = 0 and according to truth table of SR flip-flop there is no change in the output.

When inputs J = K = 0, output does not change.

Case 2 : J = 1 and K = 0

Q = 0, $\overline{Q}$ = 1 : When J = 1, K = 0 and Q = 0, S = 1 and R = 0. According to truth table of SR flip-flop it is **set** state and the output Q will be 1.

Q = 1, $\overline{Q}$ = 0 : When J = 1, K = 0 and Q = 1, S = 0 and R = 0. Since SR = 00, there is no change in the output and therefore, Q = 1 and $\overline{Q}$ = 0.

The inputs J = 1 and K = 0, makes Q = 1, i.e. **set** state.

Case 3 : J = 0 and K = 1

Q = 0, $\overline{Q}$ = 1 : When J = 0, K = 1 and Q = 0, S = 0 and R = 0. Since SR = 00, there is no change in the output and therefore, Q = 0 and $\overline{Q}$ = 1.

Q = 1, $\overline{Q}$ = 0 : When J = 0, K = 1 and Q = 1, S = 0 and R = 1. According to truth table of SR flip-flop it is a **reset** state and the output Q will be 0.

The inputs J = 0 and K = 1, makes Q = 0, i.e., **reset** state.

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Case 4 : J = K = 1

Q = 0, $\overline{Q}$ = 1 : When J = K = 1 and Q = 0, S = 1 and R = 0. According to truth table of SR flip-flop it is a set state and the output Q will be 1.

Q = 1, $\overline{Q}$ = 0 : When J = K = 1 and Q = 1, S = 0 and R = 1. According to truth table of SR flip-flop it is a reset state and the output Q will be 0.

The input J = K = 1, toggles the flip-flop output.

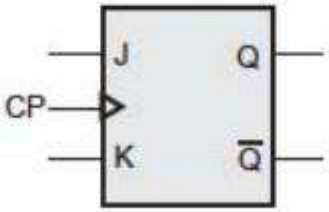

Fig. (a) Logic symbol

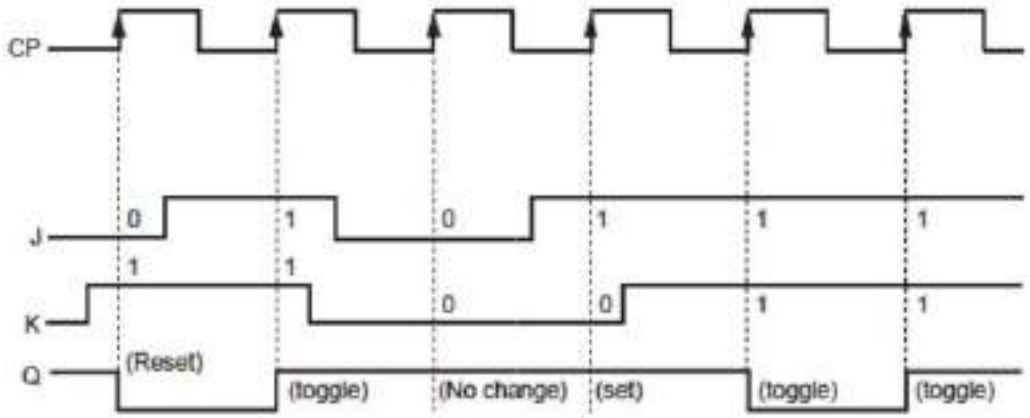

Fig. Input and output waveforms for positive edge triggered JK flip-flop

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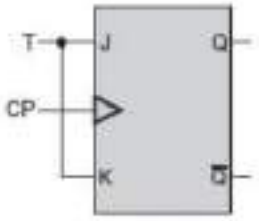
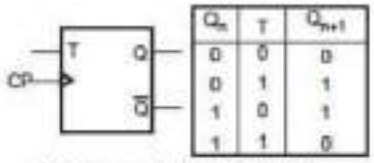
T Flip - Flop

- T flip-flop is obtained from a JK flip-flop by connecting both inputs, J and K together.
- When T = 0, J = K = 0 and hence there is no change in the output.
- When T = 1, J = K = 1 and hence output toggles.



JK to T



(a) Logic symbol b) Truth table

Fig. T Flip - flop

Shift Register

➢ ***What are shift registers ?*** **VTU : Nov.-12, May-13, Jan.-14, March-14, Marks 3**

- A group of flip-flops can be used to store a word, which is called **register**.
- The binary information (data) in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. Such registers are called '**shift registers**'.

➢ ***Explain the operational types of shift register.***

- Fig. gives the symbolical representation of the different types of data movement in shift register operations.

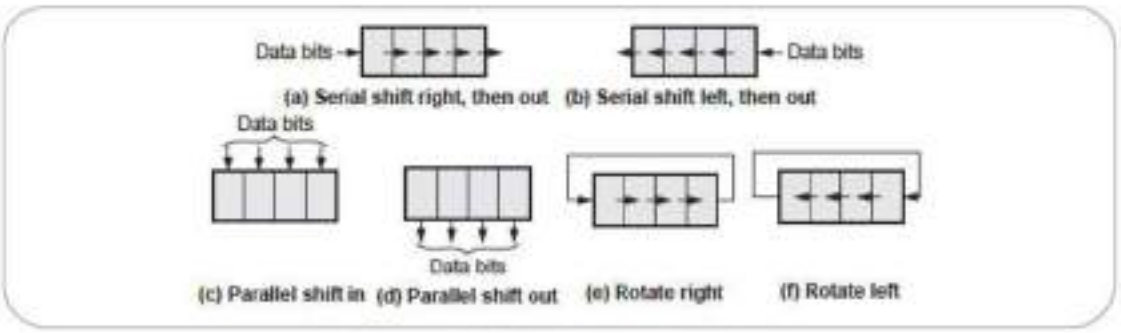


Fig. Basic data movement in registers

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➢ ***Explain the operation of SISO shift register.*** **VTU : May-14, Marks 8**

• Fig. shows serial-in serial-out shift-left register.

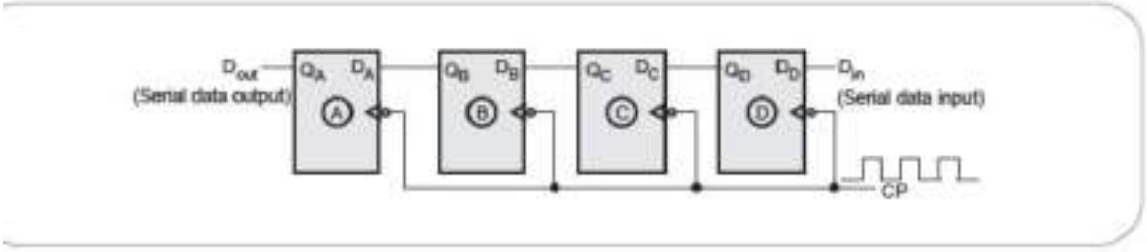

Fig. Shift-left register

• In this shift register, data within the shift register is shifted left one bit position at each clock pulse. The data input bit is loaded in the right most flip-flop.

• Fig. shows serial-in serial-out shift-right register.

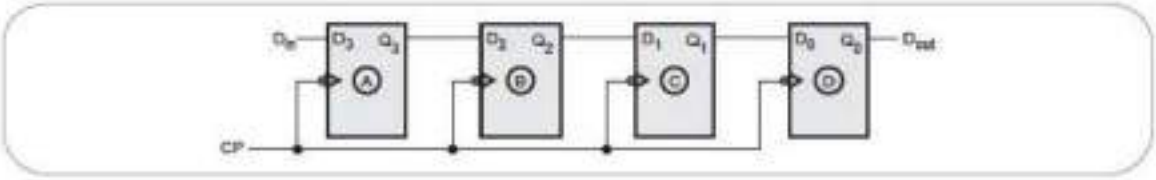

Fig. Shift-right register

• In this shift register, data within the shift register is shifted right one bit position at each clock pulse. The data input bit is loaded in the left most flip-flop.

➢ ***Explain the operation of SIPO shift register.*** **VTU : Jan.-14, Marks 4**

• In SIPO, the data bits are entered serially into the register but the output is taken in parallel.

CP	Q_3	Q_2	Q_1	Q_0
–	NC	NC	NC	NC
↓	D_3	D_2	D_1	D_0

Table Truth table

• Once the data are stored, each bit appears on its respective output line and all bits are available simultaneously as shown in Fig.

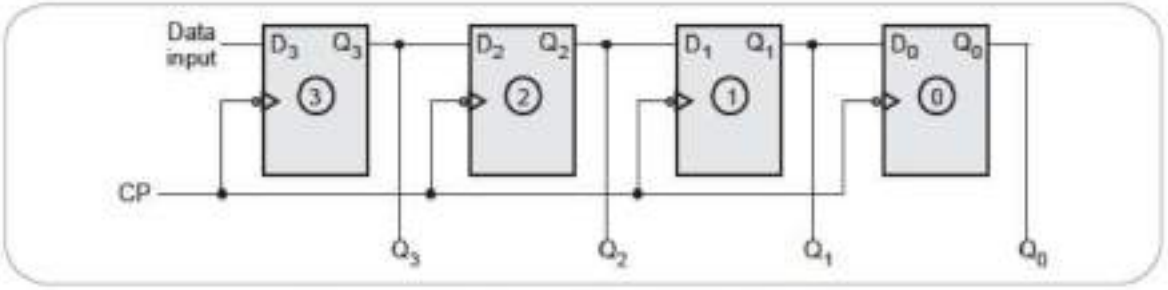

Fig. A Serial In Parallel Out (SIPO) shift register

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➢ ***Explain the operation of PISO shift register.*** **VTU : Jan.-14, Marks 4**

- Fig. illustrates a four-bit parallel in serial out register.
- There are four input lines A_3, A_2, A_1, A_0 for entering data in parallel into the register.
- SHIFT/$\overline{\text{LOAD}}$ is the control input which allows shift or loading data operation of the register.
- When SHIFT/$\overline{\text{LOAD}}$ is low, gates G_1, G_2, G_3 are enabled, allowing each input data bit to be applied to D input of its respective flip-flop.
- When a clock pulse is applied, the flip-flops with D = 1 will SET and those with D = 0 will RESET.

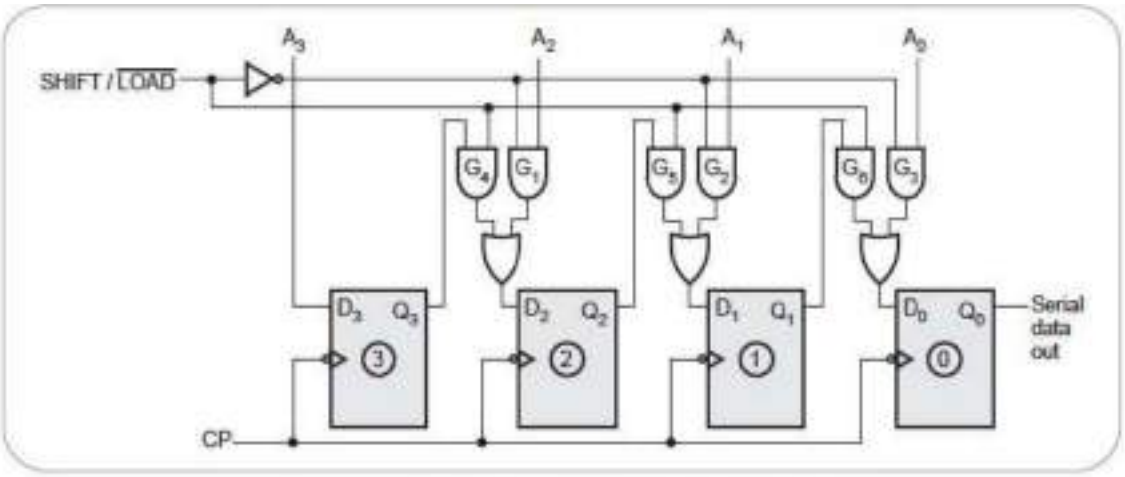

Fig. Parallel In Serial Out (PISO) shift register

- All four bits are stored simultaneously.
- When SHIFT/$\overline{\text{LOAD}}$ is high, gates G_1, G_2, G_3 are disabled and gates G_4, G_5, G_6 are enabled. This allows the data bits to shift right from one stage to the next.
- The OR gates at the D-inputs of the flip-flops allow either the parallel data entry operation or shift operation, depending on which AND gates are enabled by the level on the SHIFT/$\overline{\text{LOAD}}$ input.

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➢ *Explain parallel in parallel out shift register*

- In 'parallel in parallel out register', there is simultaneous entry of all data bits and the bits appear on parallel outputs simultaneously.
- Fig. shows this type of register.

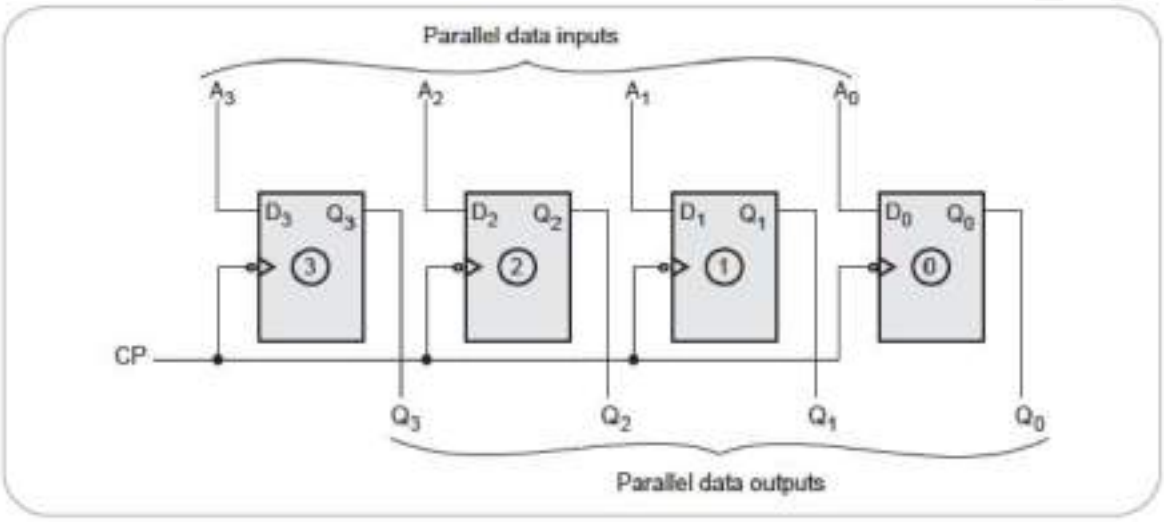

Fig. Parallel In Parallel Out (PIPO) shift register

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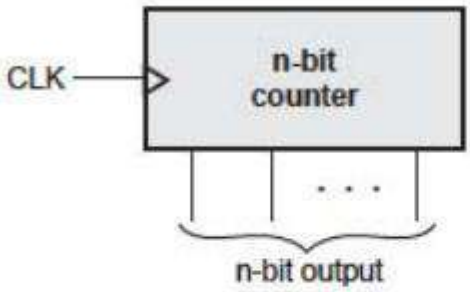
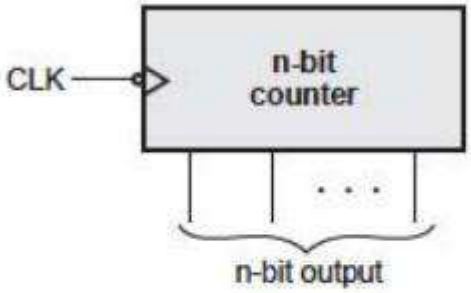
Counters

➢ *What is counter ?*

- A **counter** is a register capable of counting the number of clock pulses arriving at its clock input.
- Count represents the number of clock pulses arrived.
- On arrival of each clock pulse, the counter is incremented by one.
- In case of down counter, on arrival of each clock pulse, it is decremented by one.
- The Fig. shows the logic symbol of a binary counter.



(a) Positive edge triggered n-bit counter



(b) Negative edge triggered n-bit counter

Fig. Logic symbol of counter

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- External clock is applied to the clock input of the counter.
- The counter can be positive edge triggered or negative edge triggered.
- The n-bit binary counter has n flip-flops and it has 2^n distinct states of outputs.
- For example, 2-bit counter has
  2 flip-flops and it has $4(2^2)$ distinct states : 00, 01, 10 and 11.

- The 3-bit binary counter has 3 flip-flops and it has $8\,(2^3)$ distinct states : 000, 001, 010, 011, 100, 101 110 and 111.
- The maximum count that the binary counter can count is 2^{n-1}.
- For example, in 2-bit binary counter, the maximum count is $2^2 - 1 = 3$ (11 in binary).
- After reaching the maximum count the counter resets to 0 on arrival of the next clock pulse and it starts counting again.

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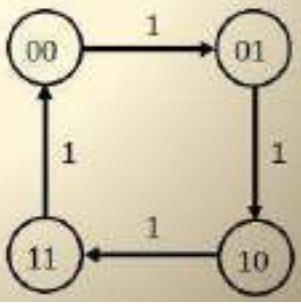
COUNTER

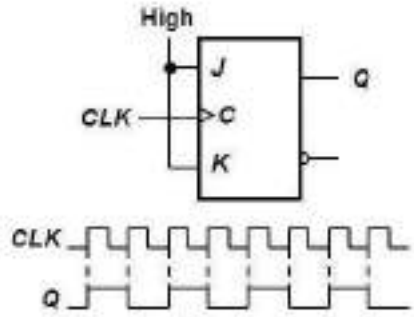
- Counters are a specific type of sequential circuit.
- The output value increases by one on each clock cycle.
- After the largest value, the output "wraps around" back to 0.
- Using two bits, we'd get something like this:

Present State A	Present State B	Next State A	Next State B
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

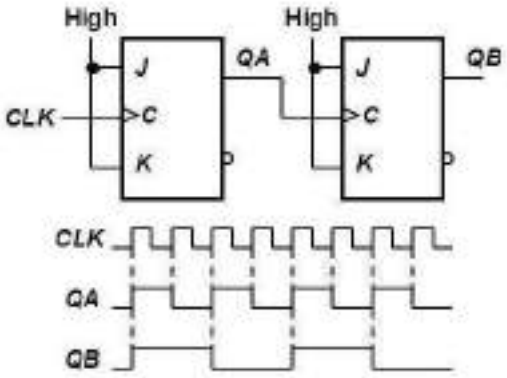


T Flip-flop

- Application: *Frequency division.*



Divide clock frequency by 2.



Divide clock frequency by 4.

- Application: *Counter*

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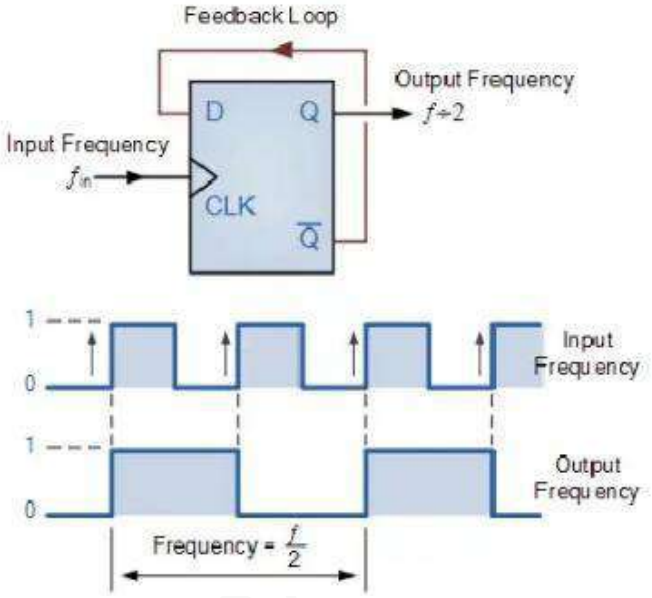
Frequency Division :

- Frequency division is one of the main propose of counters, the division process is used to reduce the frequency of the clock input waveform.



Divide by 2 counter :

- This type of counters reduces the frequency of the clock input exactly to the half for each flip-flop, this type of counters is called binary ripple counters. For n^{th} FFs , the input frequency reduces by the factor $\frac{f_{in}}{2^n}$.
- For example, the output frequency :
  - After 4 FFs $= \frac{f_{in}}{2^4} = \frac{f_{in}}{16}$
  - After 8 FFs $= \frac{f_{in}}{256}$
  - After 12 FFs $= \frac{f_{in}}{4096}$

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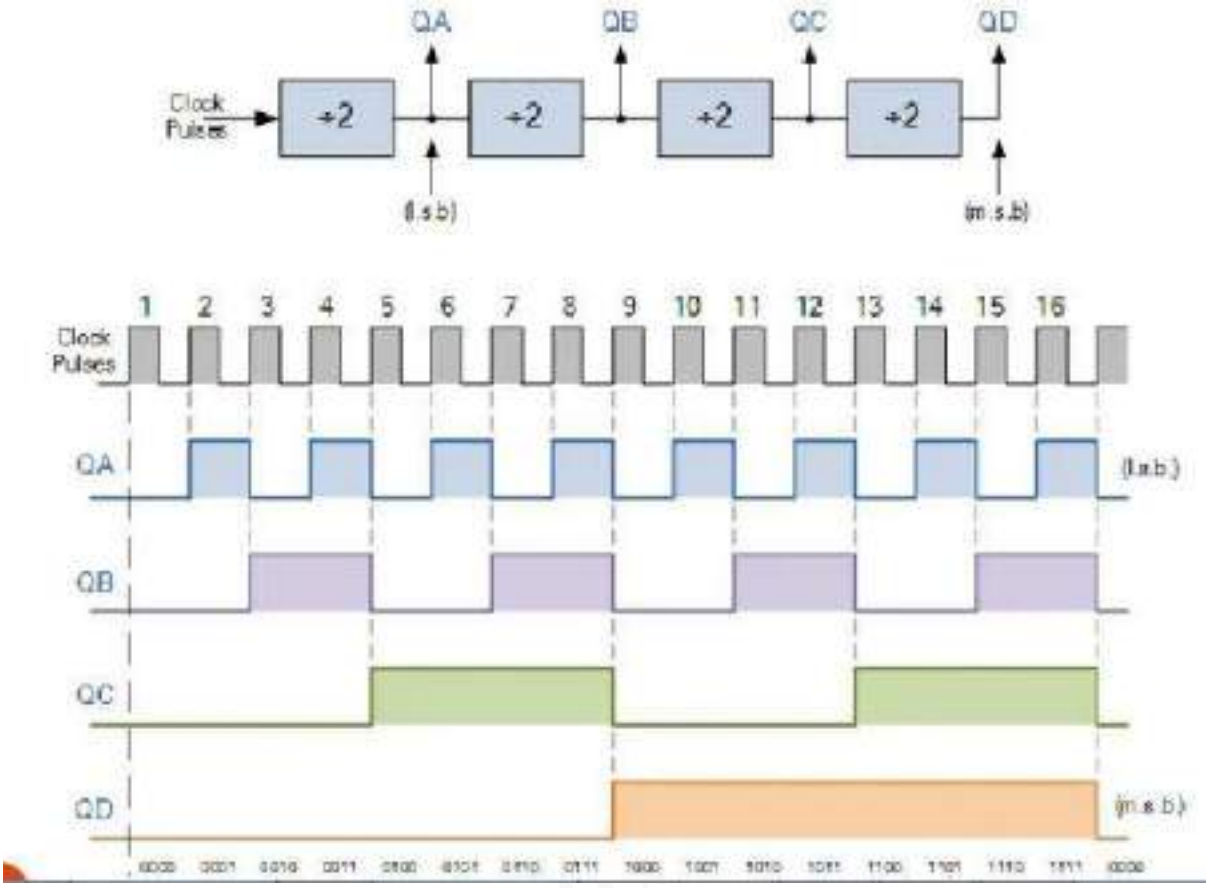

Example :

- If an input frequency of 200 KHz is applied to a binary ripple counter that has 6 FFs , what is the out put frequency of the last FF in KHz ?

- Solution :

$$f = \frac{200}{2^6} = 3.125 \text{ KHz}$$

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- Depending upon the manner in which the flip-flop are triggered, counters can be divided into two major categories.
  1) Asynchronous counter (Ripple/series counter).
  2) Synchronous counter (parallel counter).

The comparison between synchronous and Asynchronous counter.

Synchronous	Asynchronous
→ use system clock to trigger all f-f.	→ output of one used as a clock in the next f-f.
• All the flip-flops are triggered simultaneously with the same clock.	• Different FFs are triggered with different clocks.
• Operation is faster.	• Operation is slower.
• Designing is complex as the number of states increases.	• Designing is easy even for more number of states.
• Any required sequence can be designed.	• will operate only in a fixed count sequence.

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➢ *What are the type of counter ?*

- There are two types of counters : Synchronous and asynchronous (ripple).
- Table shows the comparison between synchronous and asynchronous counters.

Sr. No.	Asynchronous counters	Synchronous counters
1.	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2.	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3.	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip-flops increases in the given design.

Table Synchronous Vs Asynchronous counters

➢ *What is modulus of counter ?*

- The total number of counts or stable states a counter can indicate is called 'Modulus'.

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- The modulus of a four-stage counter would be 16_{10}, since it is capable of indicating 0000_2 to 1111_2.
- The term 'modulo' is used to describe the count capability of counters.
- For example, mod 6 counter goes through states 0 to 5 and mod 4 counter goes through states 0 - 3.

Ripple/Asynchronous Counters

➢ ***Draw and explain the working of 2-bit asynchronous binary counter.***

- Fig. (a) shows 2-bit asynchronous counter using JK flip-flops.
- The clock signal is connected to the clock input of

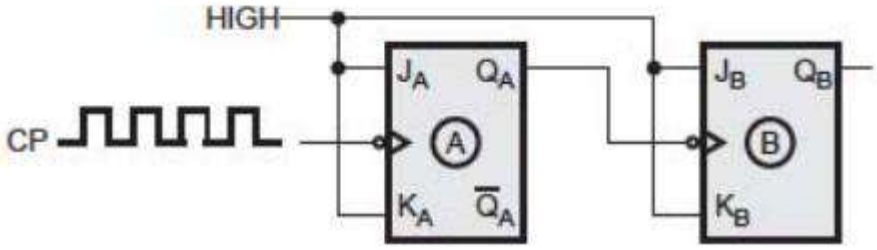

Fig. (a) A two-bit asynchronous binary counter

only first stage flip-flop.

- The clock input of the second stage flip-flop is triggered by the Q_A output of the first stage.
- Because of the inherent propagation delay time through a flip-flop, a transition of the input clock pulse and a transition of the Q_A output of first stage can never occur at exactly the same time. Therefore, the two flip-flops are never

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simultaneously triggered, which results in asynchronous counter operation.

- Fig. (b) shows the timing diagram for two-bit asynchronous counter. It illustrates the changes in the state of the flip-flop outputs in response to the clock.
- J and K input of JK flip-flops are tied to logic HIGH hence output will toggle for each negative edge of the clock input.

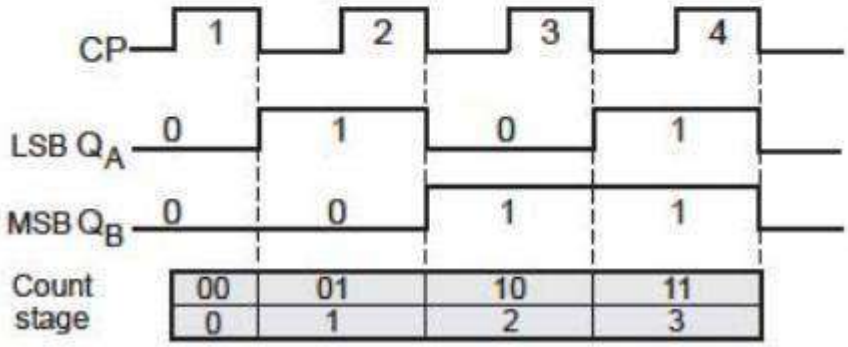

Fig. (b) Timing diagram for the counter of Fig. (a)

Modulo - 5 Ripple Counter

- For modulo ripple counter we need 3 flip - flop since $2^3 = 8 > 5$. The modulo - 5 counter will go through states : 000, 001, 010, 011 and 100. As soon as it reaches state 101 counter must reset to state 000. This reset logic is implemented by connecting NAND gate. The NAND gate produces output zero, i.e. reset signal to the flip - flop when its both inputs are logic 1. By connecting Q_0 and Q_2 output as input to NAND gate, counter gets reset when count reaches 101.

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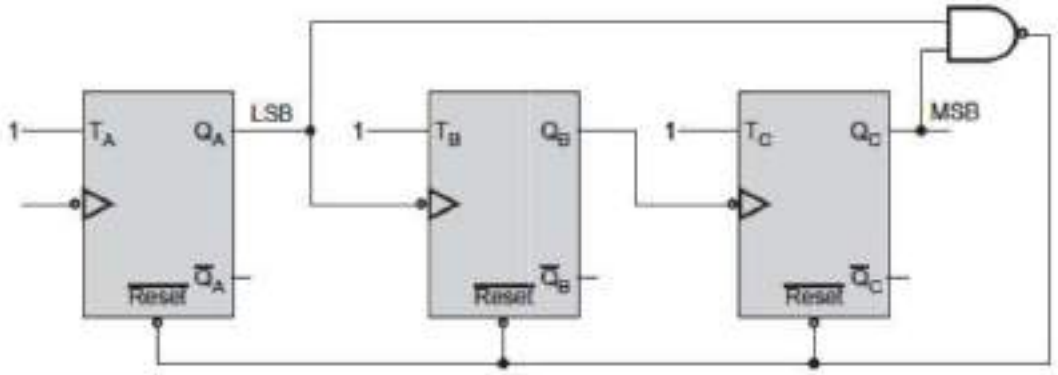

Synchronous Counter

➢ ***Draw and explain the working of 3-bit synchronous counter.*** **VTU : May-13, Marks 8**

- Fig. (a) shows 3-bit synchronous binary counter and its timing diagram.
- The state sequence for this counter is shown in Table
- Looking at Fig. (b), we can see that Q_A changes on each clock pulse as we progress from its original state to its final state and then back to its original state.
- Flip-flop A is held in the toggle mode by connecting J and K inputs to HIGH.
- Flip-flop B toggles, when Q_A is 1.
- When Q_A is 0, flip-flop B is in the no-change mode and remains in its present state.

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- Looking at the Table we can notice that flip-flop C has to change its state only when Q_B and Q_A both are at logic 1. This condition is detected by AND gate and applied to the J and K inputs of flip-flop C. Whenever both Q_A and Q_B are HIGH, the output of the AND gate makes the J and K inputs of flip-flop C HIGH and flip-flop C toggles on the following clock pulse. At all other times, the J and K inputs of flip-flop C are held LOW by the AND gate output and flip-flop does not change state.

CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table State sequence for 3-bit binary counter

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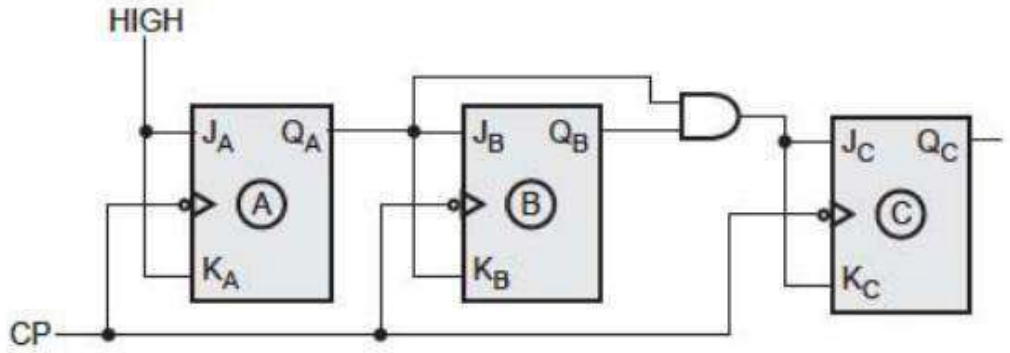
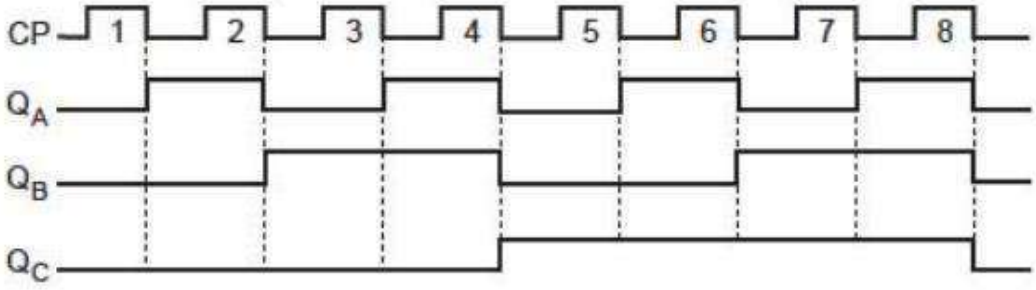


(a) A three-bit synchronous binary counter



(b) Timing diagram for 3-bit synchronous binary counter

Fig. A three-bit synchronous binary counter

Basic Communication System

➢ ***Explain the elements of communication system with the help of block diagram.***

VTU : July-16, Marks 6

- Any electronic communication system can be represented in its basic form, as shown in the Fig.

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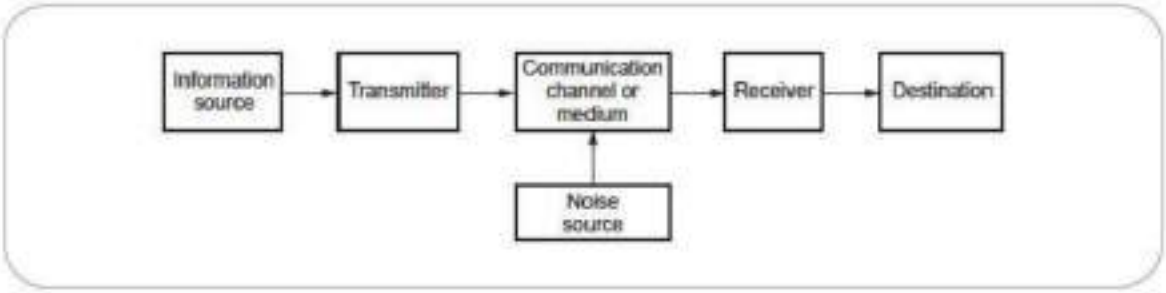

Fig. Block diagram of communication system

- The basic components of communication systems are transmitter, a communication channel or medium, and a receiver. Noise is inherently present in the channel or medium. It gets added to the information being communicated.
- The elements of communication system are as follows :
  - Information
  - Transmitter
  - Communication channel or medium
  - Noise
  - Receiver

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Information

- The communication systems communicate messages. The message comes from the information sources. The two main sources of information are the ideas emanating from the human brain and changes in any physical environment. It may contain human voice, picture, code, data, music and their combinations.
- To have a better communication system, selective, but all information must be communicated with no redundancy since we know no real information can be conveyed by a redundant message.

Transmitter

- The transmitter is a collection of electronic circuits designed to convert the information into a signal suitable for transmission over a given communication medium.

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- Most of the times message that comes from information source is non-electrical and therefore it is not suitable for immediate transmission.
- Such messages need to be coded or processed before transmission and also require suitable transducers to convert them into electrical signals. The built-in circuitry such as decoders, encoders, transducers, etc. in the transmission makes incoming information suitable for transmission and subsequent reception.
- The most of the transmitters have built-in amplifier circuits. These circuits amplify the incoming signals (information) before transmission which help in faithful reception of the transmitted information at the receiver end.

Communication channel

- The communication channel is the medium by which the electronic signal is transmitted from one place to another. The communication medium can be a pair of conducting wire, coaxial cable, optical fibre cable or free space.

Noise

- Noise is random, undesirable electric energy that enters the communication system via the medium and interferes with the transmitted message. Some noise is also produced in the receiver.
- Noise can be either natural or man-made. Natural noise includes noise produced in nature, e.g. from lighting during rainy season, or noise due to radiations produced by the sun and the other stars.

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- Man-made noise is the noise produced by electric ignition systems of cars, electric motors, fluorescent lights, etc.
- Noise is one of the serious problems of electronic communication. It cannot be completely eliminated. However, there are ways to deal with noise, and reduce the possibility of degradation of signal due to noise.

Receiver

- A receiver is a collection of electronic circuits designed to convert the signal back to the original information. It consists of amplifier, detector, mixer, oscillator, transducer and so on.

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Principle of Operations of Mobile Phone

➢ ***Define Cell, MSC and MTSO. What is roaming ?***

- A cellular/mobile system provides standard telephone operation by full-duplex two-way radio at remote locations. It provides a wireless connection to the Public Switched Telephone Network (PSTN) from any user location within the radio range of the system.
- The basic concept behind the cellular radio system is that rather than serving a given geographical area within a single transmitter and receiver, the system divides the service area into many small areas known as cells, as shown in Fig. . The typical cell covers only several square kilometres and contains its own receiver and low-power

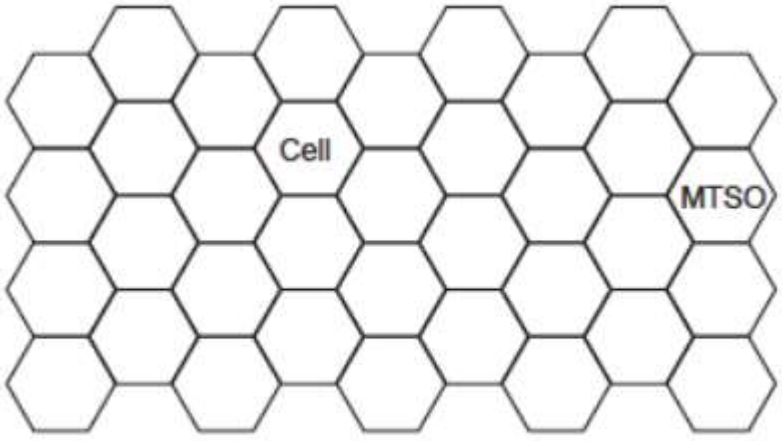

Fig. Geographic area divided into small cells

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transmitter. The cell area shown in Fig. is ideal hexagon. However, in reality they will have circular or other geometric shapes. These areas may overlap and cells may be of different sizes.

- Basic cellular system consists of mobile stations, base stations and a Mobile Switching Center (MSC). The MSC is also known as Mobile Telephone Switching Office (MTSO). The MTSO controls all the cells and provides the interface between each cell and the main telephone office. Each mobile communicates via radio with one of the base stations and may be handed off (switched from one cell to another) to any other base station throughout the duration of the call. Each mobile station consists of a transceiver, an antenna and control circuitry. The base station consists of several transmitters and receivers which simultaneously handle full duplex communication and generally have towers which

support several transmitting and receiving antennas. The base station serves as a bridge between all mobile users in the cell and connects the simultaneous mobile calls via telephone lines or microwave link to the MSC. The MSC co-ordinates the activities of all the base stations and connects the entire cellular system to the PSTN, most of the cellular system also provide a service known as **roaming.**

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Block Diagram of GSM

➢ ***Draw and explain the block diagram of GSM system ?***

- **GSM (Group of Special Mobile)** system is a second generation **(2 G)** cellular system developed in Europe. It uses **digital modulation** and **network level architectures and services.** Commercial services of GSM was started in mid-1991.
- GSM can handle both voice and data traffic.
- GSM provides subscribers with high-quality digital wireless phone service and clarity, as well as enhanced call security and privacy.
- The Fig. shows the block diagram of GSM system. It is divided into three parts :

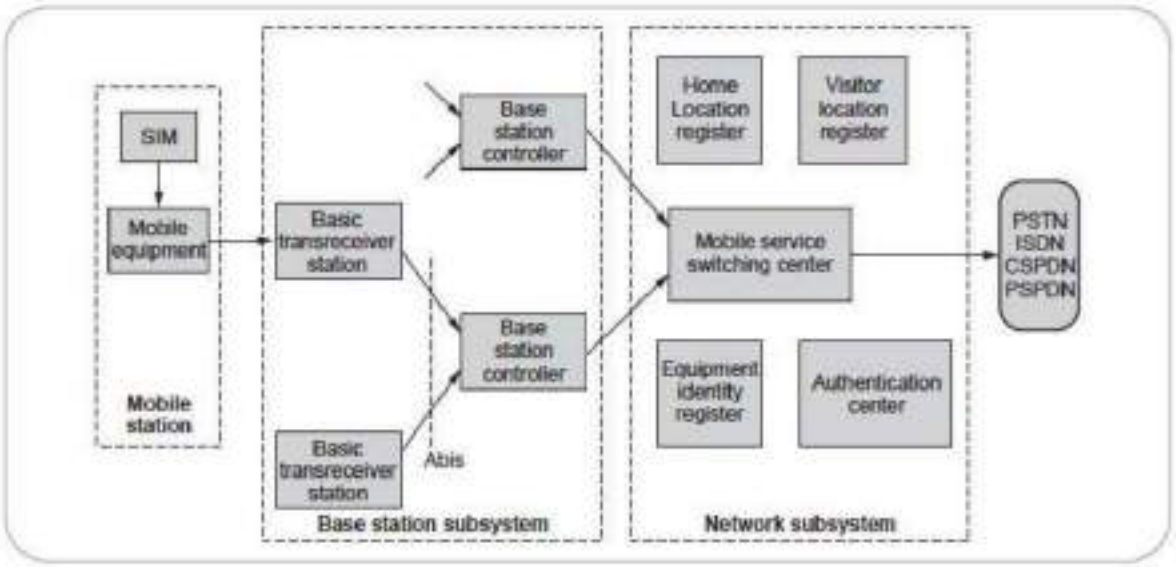

Fig. Block Diagram of GSM system

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1. Mobile station - Carried by subscriber
2. Base station sub system - Controls the radio link with mobile station
3. Network sub system - Performs switching of calls between mobile users.

Cellular Telephone Unit

➢ ***Draw and explain the block diagram of a cellular mobile radio unit.***

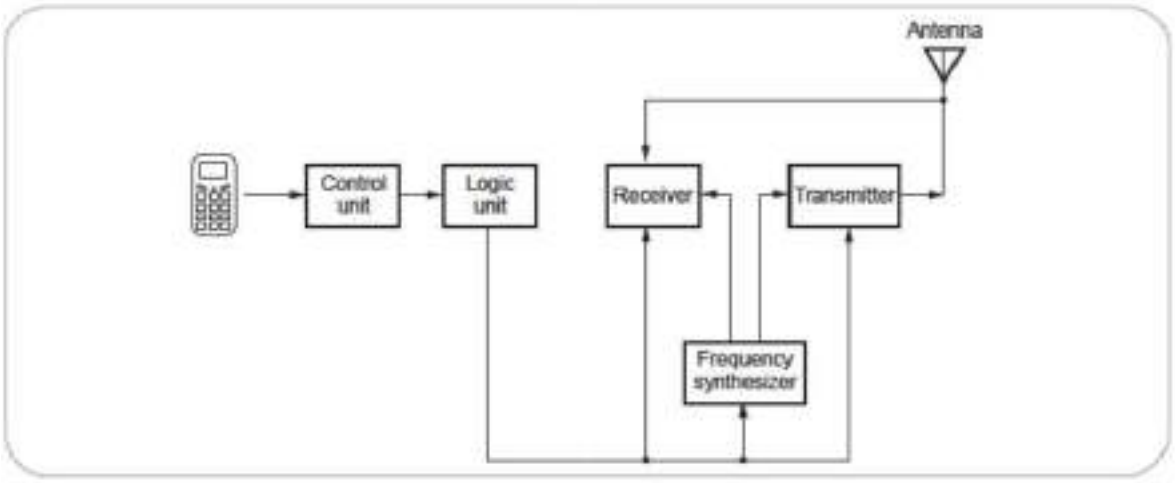

Fig. **Block diagram of a cellular radio unit**

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- Fig. shows the block diagram of a cellular mobile radio unit. As shown in the Fig. the unit consists of five major sections : transmitter, receiver, synthesizer, logic unit and control unit. The mobile unit contains built-in rechargeable batteries to provide operating power. The transmitter and receiver in the unit share the common antenna.
- It consists of RF amplifier, FM demodulator and filters. RF amplifier boosts the level of the received cell signal. Received signal is translated in the desired frequency range. It is then demodulated, filtered and amplified before being applied to the output speaker in the handset.

Transmitter

- It is a low power FM transmitter operating in the frequency range of 825 to 845 MHz. There are 666 30 kHz transmit channels.
- It produces a deviation of ± 12 kHz. The modulated output is translated up to final transmitter frequency with the help of mixer whose second input also comes from the frequency synthesizer.

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- A unique feature of the high power transmitter is that its output is controllable by the cell site and MTSO.

Receiver

- In cellular phone, dual-conversion superheterodyne receiver is used.

Frequency Synthesizer :

It is used to generate various frequency signals required for transmitter and receiver.

Logic Unit :

It is a microprocessor based master control unit for cellular radio. It is used to control operation of MTSO and mobile unit.

Control Unit :

It consists of set of speakers, microphone, touch tone dialing facility and memory.
